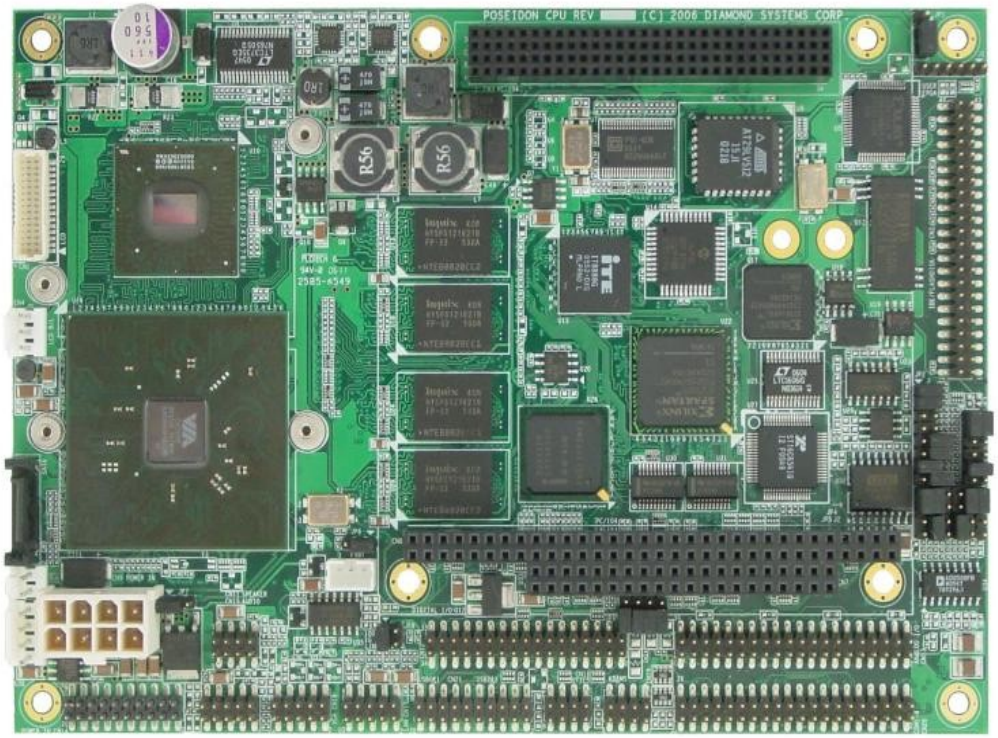
DIAMOND SYSTEMS CORPORATION

Poseidon User Manual

EPIC format VIA CPU Board with Integrated Data Acquisition

7463010 v1.2



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Introduction

Poseidon is an embedded single board computer (SBC) in an EPIC form factor that integrates CPU and data acquisition circuitry into a single board.

Poseidon conforms to the EPIC standard with expansion support via PC/104-*Plus*, an embedded standard that is based on the ISA and PCI buses and provides a compact, rugged mechanical design for embedded systems. PC/104 modules feature a pin and socket connection system in place of card edge connectors, as well as mounting holes for stand-offs in each corner. The result is an extremely rugged computer system fit for mobile and miniature applications. PC/104 modules stack together with 0.6" spacing between boards (0.662" pitch including the thickness of the PCB).

Poseidon uses the PCI bus internally to connect the Ethernet circuit to the processor. It uses the ISA bus internally to connect serial ports 3 and 4, as well as the data acquisition circuit, to the processor. Both the ISA and PCI buses are brought out to expansion connectors for the connection of add-on boards. Diamond Systems manufactures a wide variety of compatible PC/104 add-on boards for analog I/O, digital I/O, counter/timer functions, serial ports, and power supplies.

Description and Features

The Poseidon board is an all-in-one embedded SBC with the following key system and data acquisition features.

Processor Section

- Low-power, fanless 1.0GHz VIA Eden ULV CPU *or* high-performance 2.0GHz VIA C7 CPU.
- 512MB *or* 1GB 533MHz DDR2 RAM soldered, on-board, system memory.
- 400MHz front side bus.
- 2MB 16-bit wide integrated flash memory for BIOS and user programs.
- Advanced 2D/3D graphics engine with integral MPEG-2 hardware acceleration.
- 33MHz PCI Bus.

I/O Section

- 4 serial ports, 115.2kbaud max.
    - 2 ports 16550-compatible
    - 2 ports 16850-compatible with 128-byte FIFOs and RS-232, RS-422 and RS-485 capability, with RS-422/485 termination.
- 4 USB 2.0 ports.
- Accepts solid-state IDE FlashDisk modules directly on board.
- 10-/100-/1000BaseT Gigabit Ethernet.
- CRT and 24-bit dual channel LVDS flat panel support.
- Dual Independent Display.
- PS/2 keyboard and mouse ports.
- S-ATA and UDMA-100 IDE interfaces.
- Interface for amplified audio.

Analog Input

- 32 single-ended/16 differential inputs, 16-bit resolution.
- 250KHz maximum aggregate A/D sampling rate.
- Bipolar input ranges: ±10V, ±5V, ±2.5V, ±1.25V, ±0.625V.
- Unipolar input ranges: 0-10V, 0-5V, 0-2.5V, 0-1.25V, 0-.625V.
- 5 ppm/°C drift accuracy.
- Internal and external A/D triggering.
- 1024-sample FIFO for reliable high-speed sampling and scan operation.

Analog Output

- 4 analog outputs, 12-bit resolution.
- ±5V, ±10V, 0-5V, 0-10V output ranges available.
- Simultaneous update.
- Adjustable output range (optional).

Digital I/O

- 24 programmable digital I/O lines, 3.3V and 5V logic compatible.
- Enhanced output current capability: +64/-15mA max.
- Selectable pull-up/down resistors on board.

Counter/Timers

- 1 24-bit counter/timer for A/D sampling rate control.
- 1 16-bit counter/timer for user counting and timing functions.
- Programmable gate and count enable.
- Internal and external clocking capability.

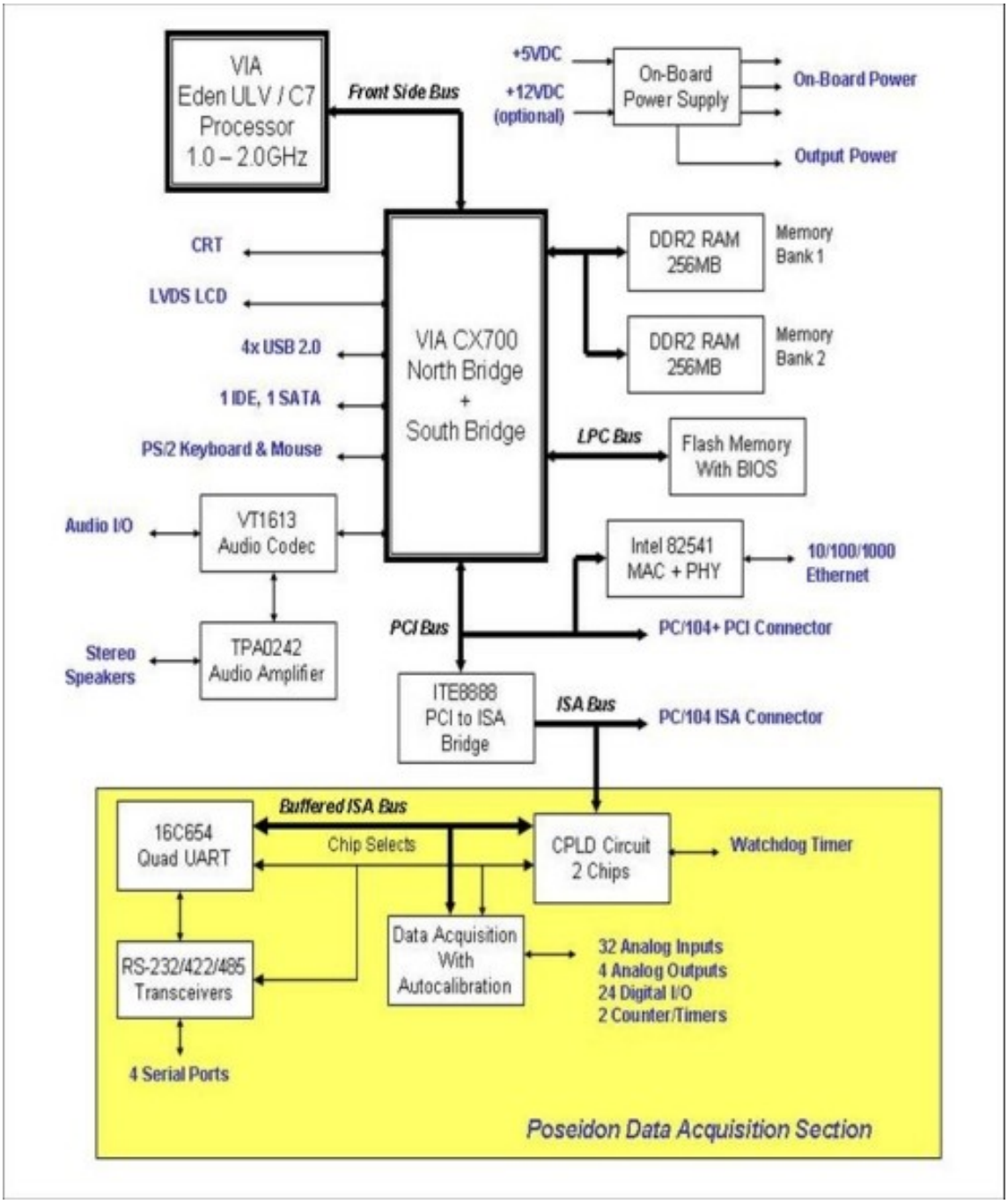
System Features

- Plug and play BIOS with IDE auto detection, 32-bit IDE access, and LBA support.
- User-selectable COM1 or COM2 terminal mode.
- On-board lithium backup battery for real-time-clock and CMOS RAM.
- ATX power switching capability.
- Programmable watchdog timer.
- I/O panel board that connects to on-board I/O brought to pin headers, to provide PC-style connectors.
- Power supply: 5VDC operation from the PC-104 bus.

Block Diagram

Figure 1 shows the Poseidon functional blocks.

Figure 1: Poseidon Functional Block Diagram



Functional Overview

This section describes the major Poseidon subsystems.

Processor

Two processor options are available for the Poseidon board.

- Low-power, fanless 1.0GHz VIA Eden ULV CPU
- High-performance 2.0GHz VIA C7 CPU

North Bridge and South Bridge

The North and South bridge are integrated in the on-board VIA CX700 chip.

Memory

The board accommodates 512MB or 1GB of SDRAM system memory soldered on the board. No expansion connector is provided for additional memory.

The board also includes flash memory for storage of BIOS and user programs. Flash memory is accessible via the on-board ISA bus.

Video Features

Video circuitry is provided by the VIA CX700 chipset and includes,

- Dual 200MHz 2D/3D graphics engines featuring dedicated 128-bit data paths for pixel data flow and texture/command access.
- An integrated MPEG-2 decoder.
- Dual independent display with separate frame buffers for CRT and flat panel displays.

Audio

The design provides AC97 audio support derived from the South Bridge chip. The Via VT1612A CODEC provides audio processing. Give special attention to design and routing to minimize noise on the audio I/O lines.

Audio I/O includes,

- Stereo line in.
- Stereo line out.
- Mono mic in.
- Stereo internal line in.

The board includes audio power amplifier circuitry for stereo speaker output. The amplifier circuit is powered by +5VDC from the board. User DC control of volume is also provided, which overrides the software settings.

Ethernet

The board supports 10-/100-/1000BaseT (Gigabit) Ethernet. Magnetics are included on the board so that a complete circuit is provided.

Data Acquisition

The board provides the following data acquisition capabilities.

Type of I/O	***Characteristics***
Analog Input	32 single-ended/16 differential inputs,16-bit resolution
Analog Output	Four analog outputs, 12-bit resolution
Digital I/O	24 programmable digital I/O, 3.3V and 5V logic compatible
Counter/Timers	One 24-bit counter/timer for A/D sampling rate control One 16-bit counter/timer for user counting and timing functions

Standard Peripherals

The board provides the following standard system peripherals.

Peripheral	***Characteristics***
Serial ports	Four serial ports
PS/2 ports	Keyboard and mouse
USB ports	Four USB 2.0 function ports
IDE ports	One 44-pin connector for HDD or FlashDisk Compact flash socket One standard S-ATA connector for up to two S-ATA HDD

Serial ports 3 and 4 can be BIOS-selected for RS-232, RS-485 or RS-422. Termination resistors of 120 ohms can be jumper-enabled on these two ports.

Console redirection feature is incorporated. This feature enables keyboard input and character video output to be routed to one of the serial ports.

The board contains provision for mounting a solid state IDE flashdisk module with capacities ranging from 32MB and greater. The module mounts onto the board using a 44-pin 2mm pitch header and a hold-down mounting hole with spacer and screws.

Bus Interfaces

The PCI bus is the primary connection between the North/South bridge, Ethernet, and PC/104-*Plus* devices.

The ISA bus is exposed on PC/104 connectors for use by add-on modules. The PC/104-*Plus* connectors allow expansion above the board only.

Power Supply

The power supply is an on-board converter, allowing an input range of +5VDC, ±5%. Jumper selection allows power to be taken from the PC-104 bus and not from the on-board converter.

The power supply includes ATX power switching and ACPI power management support. The master +5V input is controlled by the ATX function with an external switch input.

Battery Backup

The board includes a backup battery for CMOS RAM and real-time clock backup. The battery life is greater than four years. A connector and jumper are provided to disable the on-board battery and enable the use of an external battery, instead.

Watchdog Timer

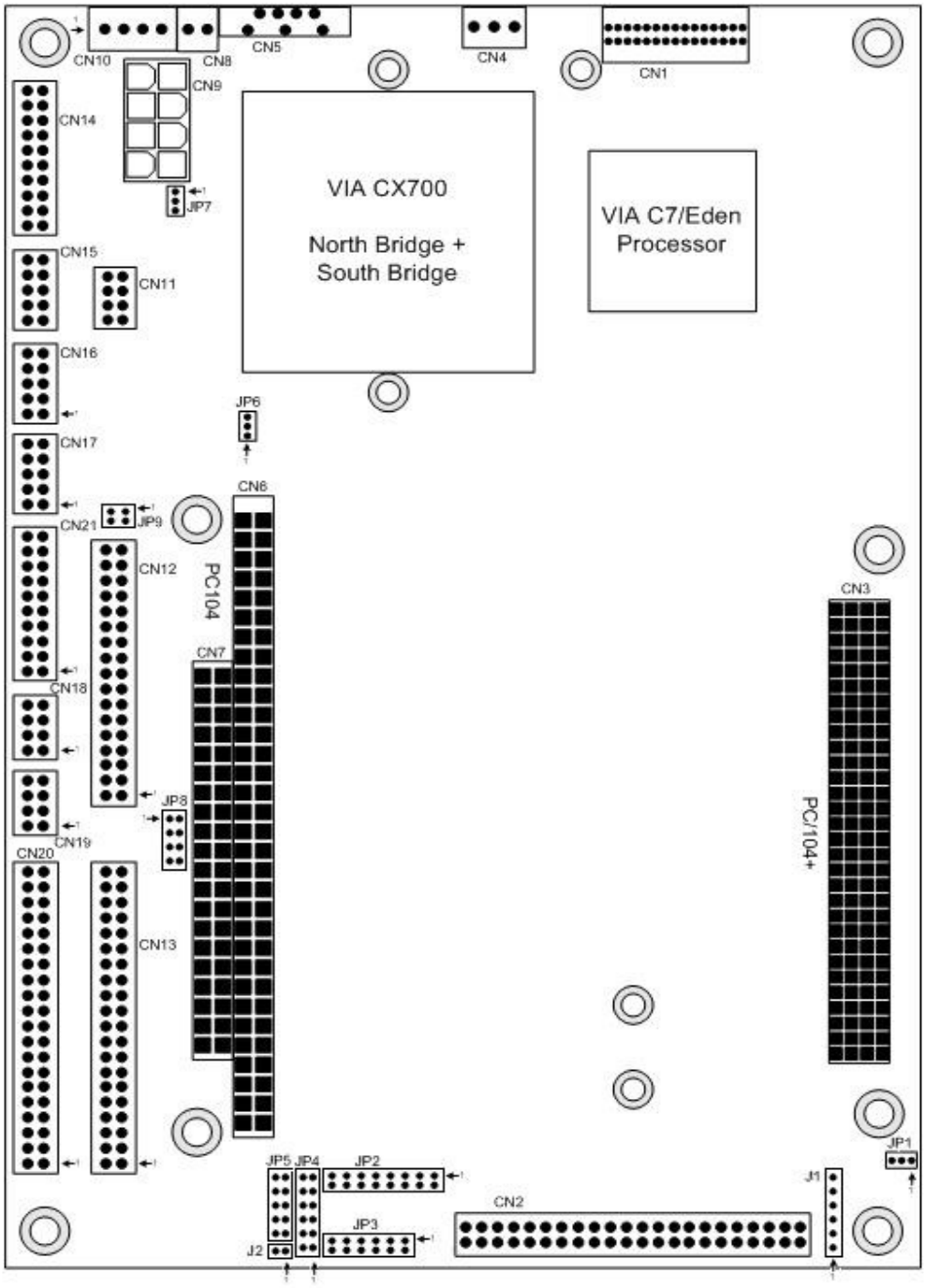
A watchdog timer (WDT) circuit consists of a programmable timer.

Board Description

Board Layout

Figure 2 shows the Poseidon board layout, including connectors, jumper blocks and mounting holes.

Figure 2: Poseidon Board Layout



Connector Summary

The following table lists the connectors on the Poseidon board.

Connector	*Description*	*Manufacturer Part No.*
CN1	LCD panel (LVDS interface)	JST: BM30B-SRDS-G-TF
CN2	Primary IDE	Standard 2x22, 0.1" header
CN3	PC/104-*Plus* PCI bus connector	EPT 264-60303-02
CN4	LCD backlight	TYCO 640456-3
CN5	Serial ATA	CATCH SATA-75
CN6	PC/104, ISA bus A,B	EPT 962-40323-03
CN7	PC/104, ISA bus C,D	EPT 962-40203-03
CN8	External battery	TYCO 640456-2
CN9	Input Power	Molex 39-31-0088
CN10	External auxiliary power (output)	TYCO 640456-4
CN11	Speaker	Standard 2x4, 2mm header
CN12	Data acquisition digital I/O, 34-pin	Standard 2x17, 2mm header
CN13	Data acquisition analog I/O, 40-pin	Standard 2x20, 2mm header
CN14	I/O panel power	Standard 2x10, 2mm header
CN15	Audio I/O	Standard 2x5, 2mm header
CN16	VGA	Standard 2x5, 2mm header
CN17	Ethernet	Standard 2x5, 2mm header
CN18	Standard button/LED utility connector	Standard 2x4, 2mm header
CN19	PS/2 Mouse and keyboard	Standard 2x4, 2mm header
CN20	RS-232/RS-485/RS-422 serial I/O (COM1-4)	Standard 2x20, 2mm header
CN21	USB 0/1, USB 2/3 (USB 2.0)	Standard 2x10, 2mm header
J1	Standard JTAG interface (Factory use)	-
J2	Voltage reference test point (Factory use)	-

Jumper Summary

The following table lists the jumpers on the Poseidon board.

Jumper	*Description*
JP1	PCI voltage selection
JP2	DAQ configuration
JP3	COM3/4 and DAQ IRQ selection
JP4	DAQ single-ended/differential selection
JP5	DAC range configuration
JP6	Battery power selection
JP7	ATX power
JP8	RS-422/485 termination
JP9	DIO pull-up/pull-down configuration

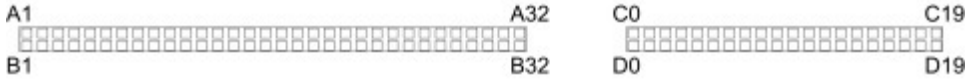
Connectors

This section describes the on-board Poseidon connectors.

PC/104 ISA Bus

Connectors CN6 and CN7 carry the ISA bus signals. Figure 3 shows the PC/104 A and B pin layout for CN6, and the C and D pin layout for CN7.

Figure 3: CN6 and CN7 Connectors



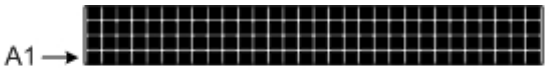
CN6 Connector Pinout			
IOCHCHK-	A1	B1	GND
SD7	A2	B2	RESETDRV
SD6	A3	B3	+5V
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	ENDXFR-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	keyed
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	REFRESH-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	+5V
SA1	A30	B30	OSC
SA0	A31	B31	GND
GND	A32	B32	GND

CN7 Connector Pinout			
GND	D0	D0	GND
SBHE-	D1	D1	MEMCS16--
LA23	D2	D2	IOCS16-
LA22	D3	D3	IRQ10
LA21	D4	D4	IRQ11
LA20	D5	D5	IRQ12
LA19	D6	D6	IRQ15
LA18	D7	D7	IRQ14
LA17	D8	D8	DACK0-
MEMR-	D9	D9	DRQ0
MEMW-	D10	D10	DACK5-
SD8	D11	D11	DRQ5
SD9	D12	D12	DACK6-
SD10	D13	D13	DRQ6
SD11	D14	D14	DACK7-
SD12	D15	D15	DRQ7
SD13	D16	D16	+5
SD14	D17	D17	MASTER-
SD15	D18	D18	GND
keyed	D19	D19	GND

PC/104-Plus PCI Bus

The PC/104-*Plus* bus is essentially identical to the PCI Bus except for the physical design. A single pin and socket connector is specified for the bus signals. A 120-pin header, J3, arranged as four 30-pin rows incorporates a full 32-bit, 33MHz PCI Bus. The additional pins on the PC/104-*Plus* connectors are used as ground or key pins. The female sockets on the top of the board enable stacking another PC/104-*Plus* board on top of the Poseidon board.

Figure 4: CN3 Connector

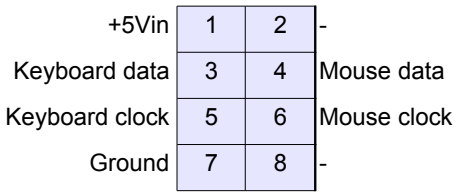


	A	B	C	D
1	GND/5.0V KEY	Reserved	+5V	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	Reserved	PAR
10	GND	PERR*	+3.3V	Reserved
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DESEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	REQ3*	GNT3*	GND/3.3V KEY

On the Poseidon, all of the PCI circuitry is driven with 3.3V circuitry and is 5V tolerant. The main board can support either 3.3V or 5V-only cards. For this reason, the connector is not keyed (to prevent certain types of cards from being inserted).

PS2 Mouse and Keyboard connector

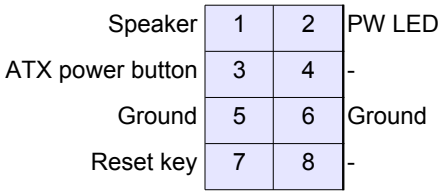
Connector CN19 is a 2x4-pin header used to connect a mouse or keyboard.



Signal	***Definition***
+5Vin	keyboard PS/2 pin 4
Keyboard data	keyboard PS/2 pin 1
Mouse data	mouse PS/2 pin 1
Keyboard clock	keyboard PS/2 pin 5
Mouse clock	mouse PS/2 pin 5
Ground	PS/2 pin 3

Utility Connector

Connector CN18 is a 2/4-pin header for access to the standard button/LED connections.



The following table describes the CN18 connector pinouts.

Signal	*Definition*
Speaker	The signal on the Speaker pin is referenced to +5V out. Connect a speaker between this pin and +5V out.
PW LED	Switched power output to connect a panel power LED. No series resistor is needed.
ATX power button	The ATX power button should be tied to ground whenever the "Power Button" is used. The "Power Button" has different functionality, depending on the current system mode and software operation. In general, the following guidelines apply. • If the board is powered down, toggling (i.e., tie to ground briefly, then release) this button turns the system on, causing all non-standby voltages to become active. **NOTE: depending on the default configuration, the system usually powers-up immediately as power is applied.** • If the system is currently powered up and active, toggling (i.e., tie to ground briefly, then release) this button causes a system power-down event to be initiated. Typically, this powers-down the monitor, hard drive, and any other non-essential functions. The system must be operating and the software executing normally for this function. Under Windows and some other OSs, this power-down event may cause the system to shut down. Typically, this is software-configurable via an option setting for the given OS. • If the system is currently powered-up and active, holding this button for four seconds causes a forced system shutdown. This is a hardware power-down, which can be detrimental to many OSs due to the fact that they are not given adequate time to initiate shut-down sequencing. This operation should only be used in critical circumstances, such as when the system itself is locked due to system instability or a software crash. After powering the system down in this manner, the system remains powered down until the power button is toggled (tied to ground again and released). When ATX is enabled, a momentary contact between this pin and Ground causes the CPU to turn on and a contact of four seconds or longer generates a power shutdown. ATX power control is enabled using a jumper on jumper block JP7.
Ground	Ground
Reset key	Connection between Reset key and ground generate a reset condition. The board remains in a reset state (with non-standby power rails disabled) until Reset key is removed from ground.

Data Acquisition (Digital I/O) Connector

Poseidon includes a 2x17-pin header, CN12, for all digital data acquisition I/O.

DIO A7	1	2	DIO A6
DIO A5	3	4	DIO A4
DIO A3	5	6	DIO A2
DIO A1	7	8	DIO A0
DIO B7	9	10	DIO B6
DIO B5	11	12	DIO B4
DIO B3	13	14	DIO B2
DIO B1	15	16	DIO B0
DIO C7	17	18	DIO C6
DIO C5	19	20	DIO C4
DIO C3	21	22	DIO C2
DIO C1	23	24	DIO C0
DIN0/CLK0	25	26	DIN1/GATE0
DOUT0/CTROUT0	27	28	DOUT2/CTROUT2
AD_RCB	29	30	DOUT1/SHOUT
DIN3/EXTCLK	31	32	DIN2/EXTGATE
+5V out	33	34	Ground

Signal	***Definition***
DIO A7-A0	Digital I/O port A; programmable direction
DIO B7-B0	Digital I/O port B; programmable direction
DIO C7-C0	Digital I/O port C; programmable direction
DIN0-1	Digital input port with counter/timer and external trigger functions
DOUT0-2	Digital output port with counter/timer functions
CLK0	Input source to Ctr 0
GATE0	Pin to control gating of Ctr 0
CROUT0	Counter 0 output
CROUT2	Counter 2 output
AD_RCB	A/D convert signal output; can be used to synchronize multiple boards
SHOUT	-
EXTCLK	External A/D trigger input; Also used for digital interrupt (DINT) input
EXTGATE	Pin to control gating of Ctrs 1& 2 for A/D timing
+5V out	Connected to switched +5V supply (Output only! Do not connect to external supply)
Ground	Digital ground (0V - reference); used for digital circuitry only

Data Acquisition (Analog I/O) Connector

Connector CN13 is a 2x20-pin header used for analog I/O data acquisition.

Single-ended

Vin 0	1	2	Vin 16
Vin 1	3	4	Vin 17
Vin 2	5	6	Vin 18
Vin 3	7	8	Vin 19
Vin 4	9	10	Vin 20
Vin 5	11	12	Vin 21
Vin 6	13	14	Vin 22
Vin 7	15	16	Vin 23
Vin 8	17	18	Vin 24
Vin 9	19	20	Vin 25
Vin 10	21	22	Vin 26
Vin 11	23	24	Vin 27
Vin 12	25	26	Vin 28
Vin 13	27	28	Vin 29
Vin 14	29	30	Vin 30
Vin 15	31	32	Vin 31
Output ground	33	34	Vout 0
Vout 1	35	36	Vout 2
Vout 3	37	38	Analog ground
DIN3/EXTCLK	39	40	Digital ground

Differential

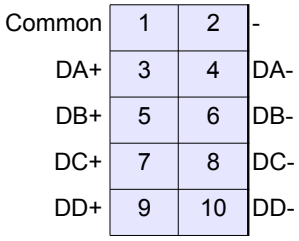
Vin 0 +	1	2	Vin 0 -
Vin 1 +	3	4	Vin 1 -
Vin 2 +	5	6	Vin 2 -
Vin 3 +	7	8	Vin 3 -
Vin 4 +	9	10	Vin 4 -
Vin 5 +	11	12	Vin 5 -
Vin 6 +	13	14	Vin 6 -
Vin 7 +	15	16	Vin 7 -
Vin 8 +	17	18	Vin 8 -
Vin 9 +	19	20	Vin 9 -
Vin 10 +	21	22	Vin 10 -
Vin 11 +	23	24	Vin 11 -
Vin 12 +	25	26	Vin 12 -
Vin 13 +	27	28	Vin 13 -
Vin 14 +	29	30	Vin 14 -
Vin 15 +	31	32	Vin 15 -
Output ground	33	34	Vout 0
Vout 1	35	36	Vout 2
Vout 3	37	38	Analog ground
DIN3/EXTCLK	39	40	Digital ground

Signal	***Definition***
Vout3-0	Analog output channels 3 – 0
Analog Ground	0V analog reference
Vin 31 ~ Vin 0	Analog input channels 31 – 0 in single-ended mode
Vin 15 + ~ Vin 0 +	High side of input channels 15 – 0 in differential mode
Vin 15 - ~ Vin 0 -	Low side of input channels 15 – 0 in differential mode
Digital ground	0V digital reference
DIN3	Digital input port with counter/timer and external trigger functions
EXTCLK	External A/D trigger input; Also used for digital interrupt (DINT) input

NOTE: The reference grounds are NOT decoupled from the power grounds – they are indirectly connected to the power supply input (and other on-board ground/0V references). Do not assume that these grounds are floating. Do not apply a high-voltage input (relative to the power input ground) to these ground signals or to any other board I/O pin.

Ethernet Connector

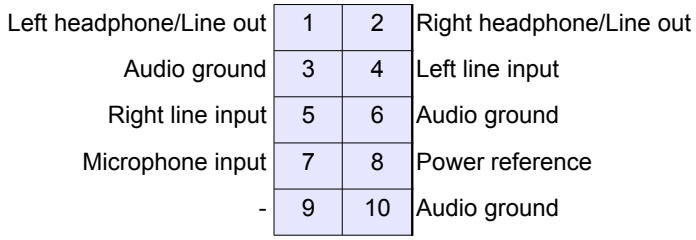
100-gigabit Ethernet connectivity is provided by connectors CN17. Connector CN17 is a 2x5-pin header.



Signal	*Definition*
DA+/-	Data A; bi-directional pair A+/A-
DB+/-	Data B; bi-directional pair B+/B-
DC+/-	Data C; bi-directional pair C+/C-
DD+/-	Data D; bi-directional pair D+/D-

Audio I/O Connector

Connector CN15 is a 2x5-pin header that provides audio connectivity.



Signal	*Definition*
Headphone/Line Out	Line Level output, capable of driving headphones, which is referred to as “Headphone Out” in most sound documentation.
Line Input	Line-Level input, which is referred to as “Line In” in most sound documentation.
Microphone Input	Microphone-level mono input; phantom power provided via pin 9.
Power reference	Microphone power reference
Audio ground	Ground

The Poseidon sound chip is AC97-compatible. The “Line Out” is powered and used for the amplified Speaker Connector output, J13, described below. The line-level output listed above is listed as either “Headphone Out” or “Line Out 2” in most of the software and documentation for this sound interface.

Speaker Connector

Connector CN11 is a 2x4-pin header used to connect speakers.

Speaker left high (+)	1	2	Speaker left low (-)
Speaker right high (+)	3	4	Speaker right low (-)
Volume, high	5	6	Volume, mid
Volume, low	7	8	-

Signal	***Definition***
Speaker LEFT +/-	Speaker Connection Pair for LEFT speaker (4-Ohm Speaker)
Speaker RIGHT +/-	Speaker Connection Pair for RIGHT speaker (4-Ohm Speaker)
Mono Output	Line-Level mono output (for reference)
Volume – LOW, MID, HIGH	These are volume controls for the attached speakers

The volume control is capable of 32 discrete levels, ranging from a 20dB maximum gain to -85dB (Muted). The main volume control is the “MID” line, which may be tied to the center tap of a potentiometer with “HIGH” on one side and “LOW” on the other to give a full range of power control.

- Shorting “MID” to “LOW” mutes the speaker audio.
- Shorting “MID” to “HIGH” provides maximum gain.
- Default (no connection) provides 10dB of gain.

The maximum output power is specified to provide up to two Watts into a 4-Ohm speaker load. Note that this output power is drawn from the on-board 5V supply.

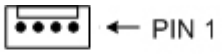
The speakers are driven using a Bridged-Tied Load (BTL) amplifier configuration. This is a differential speaker connection. As such, each speaker should be wired directly to the appropriate pair of connections for that speaker.

- Do not connect the speaker low sides (-) to ground
- Do not short the speaker low connections together.

External Auxiliary Power Connector (Output)

Connector CN10 provides switched power for use with external drives. If ATX is enabled, the power is switched ON and OFF with the ATX input switch. If ATX is not enabled, the power is switched ON and OFF in conjunction with the external power.

Figure 5: CN10 Connector



1	+5v (switched)
2	Ground
3	Ground
4	+12v (switched)

Signal	*Definition*
+5v	This is provided by the on-board power supply, derived from the input power. It is switched off when the board is powered down.
+12v	This is provided by the 12V input pin on the main power connector. It is switched off when the board is powered down.
Ground	These are 0V ground references for the power output voltage rails, above.

Cable no. 698006 mates with J15. This cable provides a standard full-size power connector for a hard drive or CD-ROM drive and a standard miniature power connector for a floppy drive.

IDE Connector

Connector CN2 is a 2x22-pin header used for the IDE connection.

Reset -	1	2	Ground
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
Ground	19	20	Key (not used)
DRQ	21	22	Ground
IDEIOW-	23	24	Ground
IDEIOR-	25	26	Ground
IORDY	27	28	Ground
DACK-	29	30	Ground
IRQ15	31	32	Pulled low for 16-bit operation
A1	33	34	Not used
A0	35	36	A2
CS1-	37	38	CS3-
LED-	39	40	Ground
+5v	41	42	+5v
Ground	43	44	Not used

Serial Port I/O Connector

Connector CN20 is a 2x20-pin header that provides access to the four on-board serial ports. The PORT1 and PORT2 serial ports are always configured for RS-232. The PORT3 and PORT4 serial ports are independently, software configurable as either RS-232, RS-485 or RS-422. All four serial ports are independently enabled.

Port No.	*Pin Assignment*
PORT1	Pins 1 - 10
PORT2	Pins 11 - 20
PORT3	Pins 21 - 30
PORT4	Pins 31 - 40

The following tables list the signals for each mode of operation, including the DE-9 pin numbers associated with the signals.

RS-232 Pin Assignment

COM1:	DCD1	1	2	DSR1
	RXD1	3	4	RTS1
	TXD1	5	6	CTS1
	DTR1	7	8	RI1
	GND	9	10	N/C
COM2:	DCD2	11	12	DSR2
	RXD2	13	14	RTS2
	TXD2	15	16	CTS2
	DTR2	17	18	RI2
	GND	19	20	-
COM3:	DCD3	21	22	DSR3
	RXD3	23	24	RTS3
	TXD3	25	26	CTS3
	DTR3	27	28	RI3
	GND	29	30	N/C
COM4:	DCD4	31	32	DSR4
	RXD4	33	34	RTS4
	TXD4	35	36	CTS4
	DTR4	37	38	RI4
	GND	39	40	-

Signal	*Definition*	*DE-9 Pin*	*Direction*
DCD*n*	Data Carrier Detect	pin 1	Input
DSR*n*	Data Set Ready	pin 6	Input
RXD*n*	Receive Data	pin 2	Input
RTS*n*	Request to Send	pin 7	Output
TXD*n*	Transmit Data	pin 3	Output
CTS*n*	Clear to Send	pin 8	Input
DTR*n*	Data Terminal Ready	pin 4	Output
RI*n*	Ring Indicator	pin 9	Input
GND	Ground	-	-

RS-485 Pin Assignment

Only CN20 connector pins 21 through 40, PORT3 and PORT4, are used for RS-485.

COM3:	NC	21	22	NC
	TXD/RXD+3	23	24	TXD/RXD-3
	GND	25	26	NC
	NC	27	28	NC
	GND	29	30	NC
COM4:	NC	31	32	NC
	TXD/RXD+4	33	34	TXD/RXD-4
	GND	35	36	NC
	NC	37	38	NC
	GND	39	40	NC

Signal	*Definition*	*DE-9 Pin*	*Direction*
TXD/RXD+*n*	Differential Transceiver Data (HIGH)	pin 2	bi-directional
TXD/RXD-*n*	Differential Transceiver Data (LOW)	pin 7	bi-directional
GND	Ground	-	-
NC	(not connected)	-	-

RS-422 Pin Assignment

Only CN20 connector pins 21 through 40, PORT3 and PORT4, are used for RS-422.

COM3:	NC	21	22	NC
	TXD+1	23	24	TXD-1
	GND	25	26	RXD-1
	RXD+1	27	28	NC
	GND	29	30	NC
COM4:	NC	31	32	NC
	TXD+2	33	34	TXD-2
	GND	35	36	RXD-2
	RXD+2	37	38	NC
	GND	39	40	NC

Signal	***Definition***	***DE-9 Pin***	***Direction***
TXD+*n*/TXD-*n*	Differential transmit data	-	Output
RXD+*n*/RXD-*n*	Differential receive data	-	Input
GND	Ground	-	-
NC	(not connected)	-	-

External Battery Connector

Connector CN8 is used to connect an external battery. The battery voltage for this input should be 3-3.5V. The current draw averages under 4µA at 3V.

Figure 6: CN8 Connector

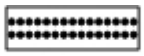
1	Battery input (+)
2	Ground

In addition to the external battery connected to CN8, the on-board battery and an additional external battery input on Utility Connector CN18 are other possible sources for maintaining the Real-Time Clock and the CMOS settings (BIOS settings for various system configurations). The battery that has the highest voltage will see the majority of the current draw, which is minimal. Note that there must be a battery voltage input for the default power-up mode.

LCD Panel (LVDS Interface) Connector

Connector CN1 provides access to the internal LVDS LCD display drivers. Note that the LCD also requires the backlight to be connected (CN4, below) to function correctly.

Figure 7: LCD Panel Connector

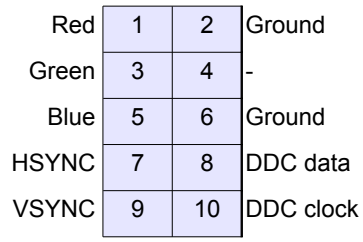


LCD1 data 0-	1	2	LCD2 data 0-
LCD1 data 0+	3	4	LCD2 data 0+
Ground	5	6	Ground
LCD1 data 1-	7	8	LCD2 data 1-
LCD1 data 1+	9	10	LCD2 data 1+
Ground	11	12	Ground
LCD1 data 2-	13	14	LCD2 data 2-
LCD1 data 2+	15	16	LCD2 data 2+
Ground	17	18	Ground
LCD1 clock-	19	20	LCD2 clock-
LCD1 clock+	21	22	LCD2 clock+
Ground	23	24	Ground
LCD1 data 3-	25	26	LCD2 data 3-
LCD1 data 3+	27	28	LCD2 data 3+
VDD (LCD display)	29	30	VDD (LCD display)

Signal	***Definition***
LCD1 Data 3-0 +/-	Primary Data Channel, bits 3-0 (LVDS Differential signaling)
LCD1 Clock +/-	Primary Data Channel, Clock (LVDS Differential signaling)
LCD2 Data 3-0 +/-	Secondary Data Channel, bits 3-0 (LVDS Differential signaling)
LCD2 Clock +/-	Secondary Data Channel, Clock (LVDS Differential signaling)
VDD	+3.3V Switched Power Supply for LCD display (only powered up when LCD display is active)
Ground	Power Ground, 0V

VGA Connector

Connector CN16 is a 2x5-pin header for connecting a VGA monitor.



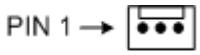
Signal	***Definition***
Red	RED signal (positive, 0.7Vpp into 75 Ohm load)
R-Ground	Ground return for RED signal
Green	GREEN signal (positive, 0.7Vpp into 75 Ohm load)
G-Ground	Ground return for GREEN signal
Blue	BLUE signal (positive, 0.7Vpp into 75 Ohm load)
B-Ground	Ground return for BLUE signal
DDCclock/data	Digital serial I/O signals used for monitor detection (DDC1 specification)
HSYNC	Horizontal sync
VSYNC	Vertical sync

Note: While the DDC serial detection pins are present, a 5V power supply is not provided (the old "Monitor ID" pins are also not used).

LCD Backlight Connector

Connector CN4 provides the backlight power and control for the optional LCD panel. See the description for connector CN1, above, for details on the LCD data interface.

Figure 8: CN4 Connector



1	+12v
2	Control
3	Ground

Signal	*Definition*
Control	Output signal (from Poseidon) to allow power-down of backlight
+12V	Power supply for LCD Backlight assembly
Ground	Ground for LCD Backlight assembly

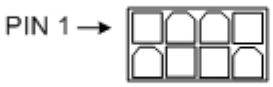
The control signal is used to allow the system to power-down the backlight when the system enables monitor-power-down during power management control.

The +12V supply is removed when the system is powered down.

Power Input Connector

The standard Poseidon input power is supplied through the CN9 connector from an external mid-range supply.

Figure 9: CN9 Connector



PS_ON	1	5	+5V standby
Ground	2	6	+5V in
Ground	3	7	+5V in
+12V in	4	8	Ground

Signal	*Definition*
+5V in	+5V main input power.
Ground	0-V (ground) power return path.
+12V in	Power supply for in-board 12V devices, including hard drives, auxiliary power, PC/104 power, and LCD backlight. Range should be 11.9V to 13.5V measured at this connector.
+5V standby	+5V standby power; powers board when in standby mode.
PS_ON	Power Supply ON. Feedback pin for external ATX supply, when needed; pulled low when on-board power is inactive.

Poseidon in the standard, mid-range power input configuration supports a voltage range from +4.75V to +5.25V, with some restrictions.

The "+12V" power supply input is intended for all on-board and board-controlled 12V power supplies, including the PC/104-*Plus* 12V supplies, the external hard drive power supply (through connector J15, described above), and the LCD backlight. If these devices are not used, the "+12V" input may be left unconnected.

Make certain that your power supply has enough current capacity to drive your system. The Poseidon requires 12 to 20 Watts or more, depending on which external devices are connected to the board. This could require over 4A on the "+Vin" line at minimum voltage inputs. In particular, many disk drives need extra current during startup. If your system fails to boot properly or if disk accesses do not work correctly, the first thing to check is the power supply voltage level. Many boot-up problems are caused simply by insufficient voltage due to excess current draw on the "+Vin" supply during initialization.

Multiple +5V and ground pins are provided for extra current carrying capacity, if needed. Each pin is rated at 3A max (15W). For the Poseidon CPU with a moderate I/O device complement (basic hard drive, key board, mouse, USB devices, and a network PC/104-*Plus* card, for example).

ATX control enables the +5V and +12V power to be switched ON and OFF with an external momentary switch. A short press on the switch turns ON power, and holding the switch on for four seconds or longer turns OFF power (See the Utility Header description for connector CN18, above).

USB 2.0 Connectors

Connector CN21 is a 2x10 pin headers for connecting USB 0/1 and USB 2/3, each providing USB 2.0 480Mbps maximum transfer rates.

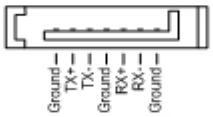
-	1	2	Shield
Shield	3	4	Shield
USB3 data+	5	6	USB2 data+
USB3 data-	7	8	USB2 data-
USB2/3 power	9	10	USB2/3 power
-	11	12	Shield
Shield	13	14	Shield
USB1 data+	15	16	USB0 data+
USB1 data-	17	18	USB0 data-
USB0/1 power	19	20	USB0/1 power

Signal	*Definition*
Shield	ground
USB0-3 power-	+5V power for USB ports 0-3
USB0-3 data+	data + for USB ports 0-3
USB0-3 data-	data - for USB ports 0-3

Serial ATA Connector

Connector CN5 is the serial ATA connector.

Figure 10: Serial ATA Connector

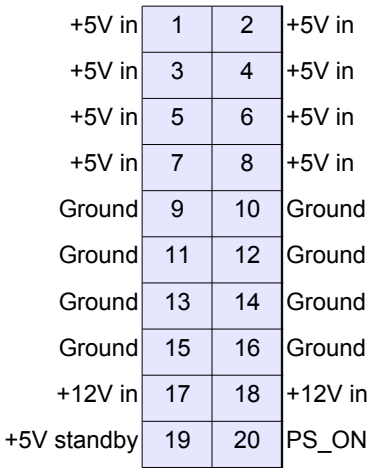


1	Ground
2	TX+
3	TX-
4	Ground
5	RX-
6	RX+
7	Ground
8	Ground
9	Ground

Signal	*Definition*
TX+/TX-	Differential outputs to PHY
RX+/RX-	Differential inputs from PHY
Ground	Ground

I/O Panel Power

Connector CN14 is a 2x10-pin header providing I/O panel power.

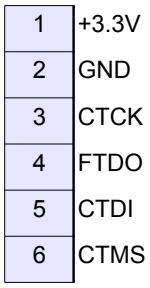


Signal	***Definition***
+5V in	+5V input
+12V in	+12V input
+5V standby	+5V standby power; powers board when in standby mode.
PS_ON	Power Supply ON. Feedback pin for external ATX supply, when needed; pulled low when on-board power is inactive.
Ground	Ground

Note: Optionally, a PC/104 power supply may be used to power the board through the PC/104 bus.

Standard JTAG Configuration Interface (Factory Use)

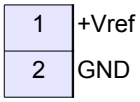
Connector J1 is the JTAG configuration interface for factory use and firmware upgrade.



Signal	*Definition*
+3.3V	Power
GND	Ground
CTCK	Test clock input
FTDO	Test data output
CTDI	Test data input
CTMS	Test mode select

Reference Voltage Test Point (Factory Use)

Connector J2 is the reference voltage test point for use during factory calibration.



Signal	*Definition*
+Vref	Reference voltage
GND	Ground

Board Configuration

Power Configurations Available:

Configuring Poseidon appropriately will guarantee your system to power on safely and reliably. This section will help you configure the board once you have selected a power configuration option.

Power can be applied in one of three different ways:

1- Via an ATX power supply using the MOLEX connector CN9 on Poseidon and cable adapter 6981091.

2- With an AC adapter such as PS-5V-04 and cable adapter 6980193 via the DB9 connector on the PNL-PSD panel board.

3- Or directly with PS-5V-04 via the MOLEX connector CN9 on Poseidon.

Additionally Poseidon provides the option of using the power button to power-up (ATX mode), or power-up as soon as power is applied (ATX Bypass).

Power Style\Power Source	**ATX PS via MOLEX**	**PS-5V-04 via Panel Board**	**PS-5V-04 via MOLEX**
Power Button (ATX)	JP7 - 2,3; JP1 - 2,3	JP7 - 2,3; JP1 - 1,2	JP7 - 2,3; JP1 - 2,3
BOOT on Power (ATX Bypass)	Not an Option	JP7 - 1,2; JP1 - 2,3	JP7 - 1,2; JP1 - 2,3; Remove Pin 5

The table summarizes the configuration for each option. JP7 refers to the ATX jumper on Poseidon while JP1 refers to the external power enable jumper on the panel board. To locate this jumper see the PNL-PSD panel board description in the final section of this manual. The table indicates the pin numbers where one jumper must be installed.

When powering the board using PS-5V-04 via the MOLEX connector and BOOT on power (ATX Bypass) is desired, the wire leading to pin 5 should be removed. If this is your definitive configuration, you might consider clipping the wire so that there is no electrical connection leading to 5Vstandby. To be certain of removing the correct lead, see the power input connector on page 30.

The Poseidon board has the following jumper-selectable configuration options.

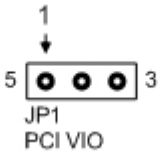
Jumper Block	***Configuration Functions***
JP1	PCI VI/O voltage setting
JP2	DAQ configuration: DMA level Base address 16/8-bit bus
JP3	COM3/COM4/ADC IRQ configuration
JP4	Analog I/O single-ended/differential configuration
JP5	DAC configuration
JP6	Battery connection (CMOS RAM erase)
JP7	ATX power
JP8	RS-422/RS-485 termination

Jumper Block	*Configuration Functions*
JP9	DIO pull-up/pull-down

PCI VI/O Voltage Setting (JP1)

JP1 provides simple access to the VIO setting for PC/104-*Plus* cards. This setting sets the voltage supplied on the "VIO" power pins of the PC/104-*Plus* connector (J3). Note that the "VIO" voltage is used on most cards to supply the I/O Voltage for all PCI signals.

Figure 11: Jumper Block JP1



JP1	
Pin Label	***Function***
3	Main +3.3v power supply on board connect pins 3-PCI VIO to select +3.3v (default configuration)
PCI VIO	PCI VIO for selecting either +3.3v or +5v onboard power supply.
5	Main +5v power supply on board connect pins 5-PCI VIO to select +5v

The Poseidon can support either I/O voltage range (all on-board signals are driven from 3.3V power rails, but are 5V tolerant), so the determination of the I/O voltage is entirely dependent on the types of PC/104-*Plus* cards plugged into the system.

PC/104-*Plus* cards should be keyed to identify the correct voltage setting. No key means that the card is universal and can accept either power setting. There are essentially 4 possibilities:

- Card keyed for 5V
- Card keyed for 3.3V
- Card not keyed – universal (can operate with either voltage setting)
- Card incorrectly keyed or not keyed but with certain requirements

The first three possibilities can be easily determined by checking the keying of the card, as shown in the following table.

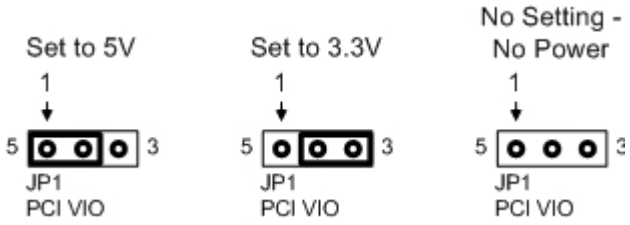
Card Voltage Type	*Pin Configuration*
5V card	Pin A1 missing/pin D30 present
3.3V card	Pin A1 present/pin D30 missing
Universal card	Pin A1 present/pin D30 present

The only solution for cards that are incorrectly keyed is to read the documentation and verify the I/O voltage (if it is called out in the card description). While not a widespread issue, this is something to be aware of when starting to work with a new PC/104-*Plus* card.

Note that this voltage selection is not used for standard PC/104 cards; only the PCI-signaling of PC/104-*Plus*.

Figure 12 shows how to select the desired voltage using jumper JP1.

Figure 12: JP1 Settings



DAQ Configuration (JP2)

Jumper block JP2 is used for base address selection, to select DMA level and to select 16- or 8-bit data bus operation.

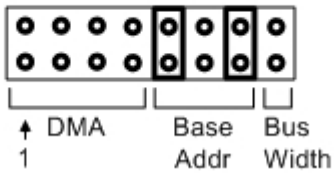
Base Address Selection

Each board in a PC/104 system must have its own unique block of addresses that does not overlap with any other board in the system or feature on the CPU. The lowest address of this address block is called the base address. The Poseidon base address is set using JP2 pins 9-14, as shown below. The table lists the possible jumper configurations, using pins 9-14, and corresponding base addresses.

Base Address	***9-10***	***11-12***	***13-14***
140h	In	In	In
340h	In	In	Out
100h	In	Out	In
180h	In	Out	Out
200h	Out	In	In
280h	Out	In	Out
300h (default)	Out	Out	In
380h	Out	Out	Out

For example, Figure 13 shows the pin configuration for base address 100h.

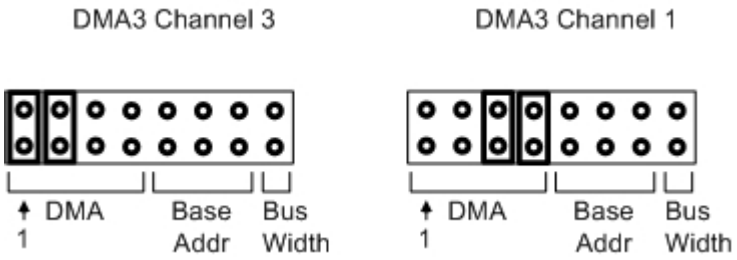
Figure 13: Base Address Configuration Example



DMA Level Selection

Jumper block JP2 contains pins for selecting the DMA level. Select either DMA channel 1 or DMA channel 3, as shown in Figure 14, below. Both pin pairs must be connected to select the desired channel.

Figure 14: DMA Channel Selection



The default configuration is no DMA and 8-bit bus width.

Note: DMA is supported in the hardware, however it is not currently supported in Diamond Systems' Universal Driver software.

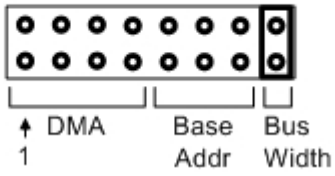
On boards without FIFOs or memory buffers, DMA is required to support high-speed sampling at rates above the maximum sustainable interrupt rate, which may vary from 1,000 to 20,000 depending on the CPU and operating system. However, Poseidon contains a 1024-sample FIFO for A/D data that allows the interrupt rate to be much slower than the sample rate. The board can support full-speed sampling at up to 250,000 samples per second without the use of DMA.

Data Bus Width Selection

The board can be configured for 16-bit read operations when reading the A/D data. To do this, jumper pins 15 and 16 on JP2. A 16-bit transfer only occurs during a 16-bit read instruction from the base address, A/D data, when the jumper is installed. Otherwise, the A/D board and host CPU ignore the 16-bit setting and/or instruction and convert the 16-bit operation into two 8-bit read operations.

Jumper pins 15 and 16, as shown in Figure 15, below, to select 16-bit operation.

Figure 15: Bus Width Configuration



COM3/COM4/ADC IRQ Configuration (JP3)

Jumper block JP3 is used to configure IRQ levels for COM3, COM4 and ADC.

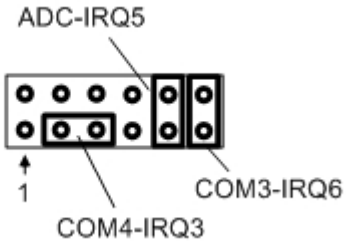
JP3	
Pin	***Function***
1	IRQ10; selectable for COM3 and COM4
2	COM3 IRQ select
3	COM4 IRQ select
4	IRQ7; selectable for COM3 and COM4
5	IRQ3; selectable for COM3 and COM4
6	COM3 IRQ select
7	COM3 IRQ select
8	IRQ4; selectable for COM3
9	IRQ5; selectable for AD and COM3
10	IRQ AD select
11	COM3 IRQ select
12	IRQ6; selectable for AD and COM3

Note: Boards Rev A1 have a different configuration table that can be found in Appendix A.

The default configuration is IRQ7 for COM3, IRQ10 for COM4 and IRQ5 for A/D.

The example in Figure 16 show the jumper settings for configuring COM4 for IRQ3, COM3 for IRQ6 and ADC for IRQ5.

Figure 16: IRQ Selection Example



Analog I/O Single-ended/Differential Configuration (JP4)

The input channels on Poseidon can be configured as 32 single-ended, 16 differential, or 16 single-ended plus 8 differential. Four different configurations are possible for the Data Acquisition (Analog I/O) connector, CN13.

A single-ended input is a single-wire input, plus ground, that is measured with reference to the board's analog ground. For accurate measurement, the board's ground must be at the same potential as the source signal's ground. Usually this is accomplished by connecting the two grounds together at some point.

A differential input is a two-wire input, plus ground, that is measured by subtracting the low input from the high input. This type of connection offers two advantages.

It allows for greater noise immunity, because the noise, which is present in equal amounts and equal phase on both the high and low inputs, is subtracted out when the low input is subtracted from the high input.

It allows for the signal to float away from ground. Normally the ground of the signal source is still connected to the ground on the A/D board in order to keep the signal from straying out of the common mode range of the A/D board's input circuitry.

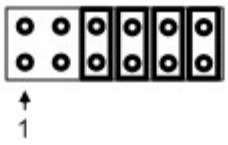
To configure the input channels, set the pin pairs in jumper block JP4 according to the table, below.

Note: For safety reasons, do not modify JP4 while the board is powered on.

Connector Pin Configuration	***1-2***	***3-4***	***5-6***	***7-8***	***9-10***	***11-12***
Inputs 0-31, single-ended (default)	In	In	Out	Out	Out	Out
Inputs 0-15, differential	Out	Out	In	In	In	In
Inputs 0-7, differential Inputs 8-15, single-ended Inputs 24-31, single-ended	Out	In	In	Out	In	Out
Inputs 0-7, single-ended Inputs 8-15, differential Inputs 16-23, single-ended	In	Out	Out	In	Out	In

For example, Figure 17 shows the JP4 jumper settings to configure CN13 pins 0-15 for differential mode.

Figure 17: Analog I/O Single-ended/Differential Configuration Example



DAC Configuration (JP5)

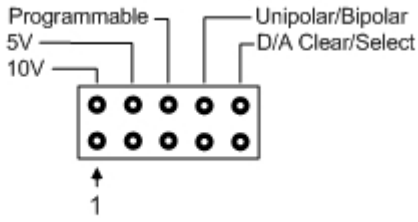
The analog outputs on Poseidon can be set to operate in bipolar (both + and –) or unipolar (+ only) output voltage ranges. In addition, the full-scale output range can be set to 5V, 10V, or programmable. The maximum output current on any channel is 5mA. Current outputs such as 0-20mA outputs are not supported.

On power-up, the DACs can be configured to reset to mid-scale (0V in bipolar mode) or zero scale (0V in unipolar mode). Generally, the reset mode should be selected so that the DACs power-up to 0V.

In programmable mode, the full-scale output voltage can be set anywhere from 0V to 10V in software. You must use the Universal Driver software to set programmable D/A range, because it requires calibration to fine-tune the setting to the desired value.

To configure the analog output range, set jumper block JP5 according to the tables below. The first four positions are used for the output range, and the fifth position is for the power-up reset mode.

Figure 18: JP5 Jumper Block



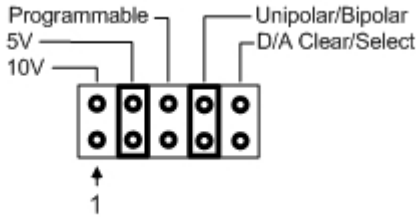
Output Range	*10V*	*5V*	*Programmable*	*Polarity*	*D/A Clear/Select*
±5V	Out	In	Out	In	X
±10V	In	Out	Out	In	X
0-5V	Out	In	Out	Out	X
0-10V	In	Out	Out	Out	X
Programmable, unipolar	Out	Out	In	Out	X
Programmable, bipolar	Out	Out	In	In	X

Note: Programmable mode requires use of driver software to set and calibrate range.

The default configuration is 5V, unipolar.

Figure 19 shows the JP5 configuration for setting the output range to ±5V.

Figure 19: D/A Configuration for ±5V Output Range Example

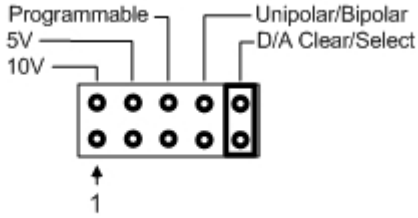


The following table shows the jumper position for power-up reset mode.

Output Range	*10V*	*5V*	*Programmable*	*Polarity*	*D/A Clear/Select*
Mid-scale, bipolar modes	X	X	X	X	Out
Zero scale, unipolar modes	X	X	X	X	In

Figure 20 shows the jumper setting to configure the DACs to reset to zero scale. (Omit the jumper to reset to mid-scale).

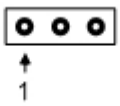
Figure 20: D/A Configuration to Reset to Zero Scale Example



Battery Connection (JP6)

The CMOS RAM may be cleared using the 3-pin JP6 jumper block. By default, there are jumpers on pins one and two for standard BIOS configuration.

Figure 21: JP6 Jumper



With the jumper in position 1-2, the CPU powers up with the default BIOS settings. Follow these steps to clear the CMOS RAM.

1. Power-down the CPU.
2. Remove the jumper from position 1-2.
3. Insert the jumper in position 2-3.
4. Wait a few seconds.
5. Insert the jumper in position 1-2.
6. Power-up the CPU.

Note: Before erasing CMOS RAM, write down any custom BIOS settings.

ATX Power Control (JP7)

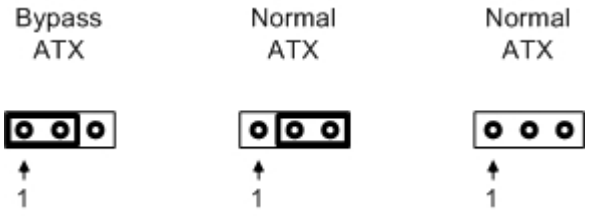
The ATX power control is set using the JP7 ATX jumper block. ATX power control has the following behavior.

- If the ATX jumper is out, ATX works normally and an external, momentary switch may be used to turn power ON and OFF. A quick contact turns the power ON, and a long contact (greater than four seconds) turns the power OFF.
- If the ATX jumper is in, the ATX function is bypassed and the system powers up as soon as power is connected.

If the ATX jumper is removed, the battery-backup for CMOS and the real-time clock settings do not function when power is removed.

Figure 18 shows the ATX configuration options using the JP7 jumper block. (Pin 3 is not connected).

Figure 22: ATX Configuration Using JP7

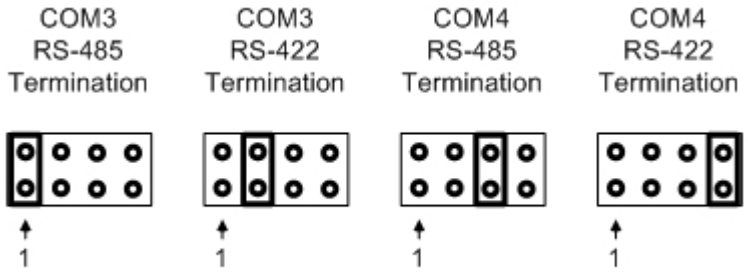


The default configuration is ATX bypass.

RS-422/RS-485 Termination Configuration (JP8)

If the Poseidon board is the last card in a RS-422/RS-485 link, the link must be terminated. Use jumper block JP9 to terminate RS-422 and RS-485 lines for COM3 and COM4. Figure 21 shows the termination configuration options.

Figure 23: RS-422/RS-485 Termination Configuration Options

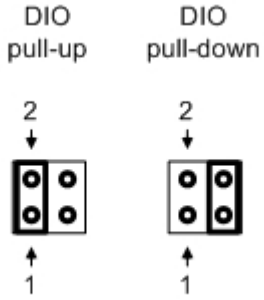


The default configuration is no termination.

DIO Pull-up/Pull-down Configuration (JP9)

Configure the DIO lines for pull-up or pull-down using jumper block JP8, as shown in Figure 22.

Figure 24: DIO Pull-up/Pull-down Configuration



By default, the lines will be pulled high.

System Features

System Resources

The table below lists the default system resources utilized by the circuits on Poseidon.

Device	*Address*	*ISA IRQ*	*ISA DMA*
Serial Port COM1	I/O 0x3F8 – 0x3FF	4	–
Serial Port COM2	I/O 0x2F8 – 0x2FF	3	–
Serial Port COM3	I/O 0x3E8 – 0x3EF	7	–
Serial Port COM4	I/O 0x2E8 – 0x2EF	10	–
IDE Controller	I/O 0x1F0 – 0x1F7	14	–
A/D Circuit (when applicable)	I/O 0x140 – 0x380	5	–
Serial Port / FPGA Control	I/O 0xA50-0xA5F	–	–
Ethernet	OS-dependent	OS-dependent	–
USB	OS-dependent	OS-dependent	–
Sound	OS-dependent	OS-dependent	–
Video	OS-dependent	OS-dependent	–

Most of these resources are configurable and, in many cases, the Operating System alters these settings. The main devices that are subject to this dynamic configuration are on-board Ethernet, sound, video, USB, and any PC/104-*Plus* cards that are in the system. These settings may also vary depending on what other devices are present in the system. For example, adding a PC/104-*Plus* card may change the on-board Ethernet resources.

The serial port settings for COM3 and COM4 are jumper selectable, whereas the settings for COM1 and COM2 are entirely software-configured in the BIOS.

Console Redirection to a Serial Port

In many applications without a local display and keyboard, it may be necessary to obtain keyboard and monitor access to the CPU for configuration, file transfer, or other operations. Poseidon supports this operation by enabling keyboard input and character output onto a serial port, referred to as console redirection. A serial port on another PC can be connected to the serial port on Poseidon with a null modem cable, and a terminal emulation program, such as HyperTerminal, can be used to establish the connection. The terminal program must be capable of transmitting special characters including F2 (some programs or configurations trap special characters).

The default Poseidon BIOS setting enables console redirection onto COM2 during power-on self-test (POST). Communication parameters are 115.2Kbaud, N, 8, 1. When the CPU is powered up, the BIOS outputs POST information to COM2 and monitors the port it for any keyboard activity. You can enter the BIOS by pressing F2 during this time interval. In the default configuration, console redirection is disabled after POST is finished and the CPU boots.

There are three possible configurations for console redirection:

- POST-only (default)
- Always On
- Disabled

To modify the console redirection settings,

1. Enter the BIOS

2. Select the Advanced menu

3. Select Console Redirection.

4. In Com Port Address, select Disabled to disable the function, On-board COM A for COM1, or On-board COM B for COM2 (default).

   If you select Disabled, you will not be able to enter BIOS again during power-up through the serial port.

To reenter BIOS when console redirection is disabled, you must either install a PC/104 video board and use a keyboard and terminal or erase the CMOS RAM, which will return the BIOS to its default settings. CMOS RAM may be erased by removing the jumper on the JP6 jumper block.

Note: Before erasing CMOS RAM, write down any custom BIOS settings you have made.

If you erase the CMOS RAM, the next time the CPU powers up COM2 returns to the default settings of 115.2Kbaud, N, 8, 1 and operates only during POST.

If you selected COMA or COMB, continue with the configuration, as follows.

1. For Console Type, select PC ANSI.

2. You can modify the baud rate and flow control here if desired.

3. At the bottom, for Continue C.R. after POST, select Off (default) to turn off after POST or select On to remain on always.

4. Exit the BIOS and save your settings.

Flash Memory

Poseidon contains a 2Mbyte, 16-bit wide flash memory chip for storage of BIOS and other system configuration data.

Backup Battery

Poseidon contains an integrated RTC/CMOS RAM backup battery. This battery has a capacity of 120mAH and will last over three years in power-off state. There is also a connection points for alternative, external battery power on header CN8.

The external battery should be 3-3.6V and should be able to provide a continuous supply with a nominal 2uA continuous current drain and a peak short-term drain of 1mA. An external battery is only recommended where concern for on-board CMOS settings and/or time accuracy make such redundancy worthwhile.

The on-board battery is activated for the first time during initial factory configuration and test.

System Reset

Poseidon contains a chip to control system reset operation. Reset occurs under the following conditions.

- User causes reset with a ground contact on the *Reset* input.
- Input voltage drops below 4.75V.
- Over-current condition on output power line .

The ISA Reset signal is an active high pulse with a 200ms duration. The PCI Reset is active low, with a typical pulse width duration of 200 msec.

On-Board Video

Using the the on-board VIA CX700 processor, Poseidon integrates all of the support needed for modern media. Refer to the VIA Technologies, Inc. documentation for CX700-series processors, listed in the Additional Information section of this document.

System I/O

Ethernet

Poseidon includes a 10/100/1000 BaseT (Gigabit) Ethernet connectivity, using an Intel 82541 Gigabit Ethernet controller. The signals are provided on two connectors on the right edge of the board:

Jumper Block	*Connector Type*
J10	RJ45
J11	6-pin header

Serial Ports

Poseidon contains four serial ports. Each port is capable of transmitting at speeds up to 115.2Kbaud. Ports COM1 and COM2 are built into the standard chipset., which are standard 16550 UARTs with 16-byte FIFOs.

Ports COM3 and COM4 are derived from an Exar 16C2850 dual UART chip and include 128-byte FIFOs. These ports may be operated at speeds to 1.5Mbaud with installation of high-speed drivers, as a custom option.

The serial ports use the following default system resources.

Port	*I/O Address Range*	*IRQ*
COM1	0x3F8 - 0x3FF	4
COM2	0x2F8 - 0x2FF	3
COM3	0x3E8 - 0x3EF	7
COM4	0x2E8 - 0x2EF	10

The COM1 and COM2 settings may be changed in the system BIOS. Select the *Advanced* menu, followed by *I/O Device Configuration,* to modify the base address and interrupt level.

The settings of COM3 and COM4 I/O addresses may be changed using jumpers J5. The jumper settings are auto-detected by the BIOS.

> **Note: The IRQ settings for COM3 and COM4 are selected using jumper J4. COM3 may use IRQ4, IRQ7 or IRQ10. COM4 may use IRQ3, IRQ7 or IRQ10. Once these jumper selections are made, you must update the serial port IRQ settings in the BIOS and device driver to match these selections; the IRQ settings are NOT auto-detected in the way that the address settings are detected.**

RS-232 Mode

RS-232 mode is the standard mode for most PC applications. COM1 and COM2 are always RS-232-only. COM3 and COM4 are RS-232 by default and the settings are managed in the BIOS using the *I/O Device Configuration* menu.

RS-232 mode for all four ports provides complete signaling support, including all handshaking signals and the Ring Indicate (RI) signal.

RS-485 Mode

COM3 and COM4 are independently selectable between RS-232 mode (default) and RS-485 mode. If RS-485 mode is selected, special consideration is required to implement RS-485 mode in both hardware and software.

In hardware, the critical issues for RS-485 mode are:

- Receive and transmit only. No handshaking lines are supported.
- Differential signaling; two wires each, high and low, for receive and transmit.
- Signal definitions for connector J18 change depending on the mode for each serial port.

In software, control of the RS-485 transmit line is handled using the serial port RTS signal. Defined as a handshaking signal for RS-232, it is used as a write-control signal for RS-485 operation.

The RS-485 implementation for COM3/4 always receives the data sent. For example, when data is transmitted from COM3, the same data is locally echoed back into the receive buffer of COM3. This allows for data verification to identify RS-485 network collisions; i.e., if another device sends data onto the RS-485 lines at the same time, the data coming into the receive buffer does not match and is not received.

To transmit data for one of these RS-485 ports, the RTS signal must be driven active. The transmitter for that RS-485 port is then active and remains active until the RTS signal is returned to its default, no-transmit, state.

The typical sequence to transmit data on a shared RS-485 cable as follows.

1. Set RTS high to enable transmit.
2. Send data, which is echoed to the receive buffer of the same port.
3. Set RTS low to disable transmit.
4. Verify that data is received and that it matches the transmit data. If the data does not match, re-transmit the data.

RS-422 Mode

COM3 and COM4 are independently selectable to operate in RS-422 mode, instead of RS-232 mode (default) or RS-485 mode. Jumper the J4 connector RS-422 pins to override the BIOS RS-232/RS-485 selection. To operate COM3 in RS-422 mode, jumper J4 pins labeled *C3 422*. To operate COM4 in RS-422 mode, jumper J4 pins labeled *C4 422*.

If RS-422 mode is selected, special hardware and software consideration is required to implement RS-422.

PS/2 Ports

Poseidon supports two PS/2 ports.

- Keyboard
- Mouse

The PS/2 ports are accessible using a cable assembly (DSC# **6981022**) attached to connector J6. Support for these ports is independent of, and in addition to, mouse and keyboard support using the USB ports.

USB Ports

Four USB 2.0 ports, USB0 through USB3, are accessible using cable assemblies attached to connector CN21.

USB support is intended primarily for the following devices (although any USB-standard device should function).

- Keyboard
- Mouse
- USB Floppy Drive (This is required for Crisis Recovery of boot ROM)
- USB flash disk

The BIOS supports the USB keyboard during BIOS initialization screens and legacy emulation for DOS-based applications.

The USB ports can be used for keyboard and mouse at the same time that the PS/2 keyboard and mouse are connected.

Data Acquisition Circuit

Poseidon integrated data acquisition functions incorporate the same circuitry as the DMM-32X-AT PC/104 module. Poseidon utilizes Diamond Systems' patented Automatic Auto-calibration technology to calibrate the A/D and D/A circuits automatically when required, without user intervention. Auto-calibration provides analog I/O performance with the maximum possible accuracy over the life of the product.

If using Diamond Systems Universal Driver (DSCUD), develop code in the same way as for the DMM-32X-AT. The code developed for the DMM-32X-AT runs with no change on Poseidon, with the exception that the Poseidon DAQ does not have an equivalent to the DMM-32X-AT serial port.

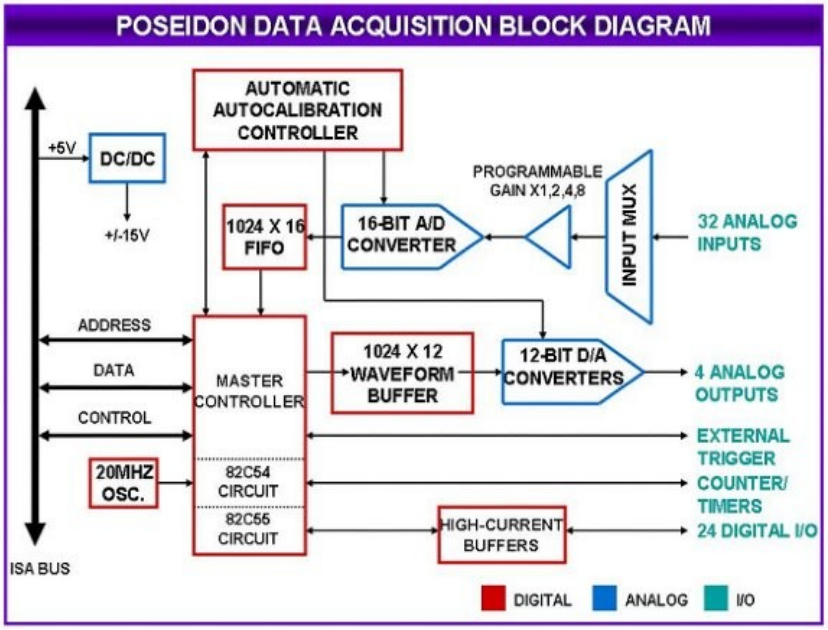
Poseidon has the following Data Acquisition Circuit features.

- 32 analog inputs with 16-bit A/D and 250KHz sample rate
- 4 analog outputs with 12-bit D/A and 100KHz waveform output capability
- 24 digital I/O lines
- 2 counter/timers
- interrupt and DMA A/D transfers, using an enhanced 1,024-sample FIFO with programmable threshold

Note: Diamond Systems free Universal Driver software for Linux, Windows 98/2000/XP/CE.NET, DOS, QNX, and VxWorks is available for programming the board.

Figure 25 shows a block diagram of the data acquisition circuit.

Figure 25: Data Acquisition Block Diagram



Data Acquisition Circuitry I/O Map

I/O Memory Space

Poseidon occupies 16 bytes in the system I/O address space. Registers 12 through 15 provide paged windows for access to additional registers without requiring additional I/O address space.

The following tables list the register functions and base address offset, for each page.

Note: Control bits in register 8 are used for page selection.

Main Register Set		
Base +	***Write Function***	***Read Function***
0	Start A/D Conversion	A/D LSB (bits 7-0)
1	Auxiliary Digital Output	A/D MSB (bits 15-8)
2	A/D Low Channel	A/D low Channel Read-back
3	A/D high Channel	A/D high Channel Read-back
4	DAC LSB	Status/Auxiliary Digital Input
5	DAC MSB + Channel	FIFO Threshold Read-back (bit 8)
6	FIFO Threshold	FIFO Threshold Read-back (bits 7-0)
7	FIFO Control	FIFO Status
8	Miscellaneous and Page Control	A/D Status
9	Interrupt and A/D Clock Control	Interrupt and A/D Clock Status
10	Counter/Timer and DIO Control	C/T and DIO Control Read-back
11	Analog Configuration	Analog I/O Read-back

Page 0 - 82C54 Counter/Timer Access		
Base +	***Write Function***	***Read Function***
12	Counter 0 Data	Counter 0 Data Read-back
13	Counter 1 Data	Counter 1 Data Read-back
14	Counter 2 Data	Counter 2 Data Read-back
15	82C54 Control	82C54 Control Read-back

Page 1 - 82C55-Type Digital I/O		
Base +	***Write Function***	***Read Function***
12	DIO Port A Output	DIO Port A Input
13	DIO Port B Output	DIO Port B Input
14	DIO Port C Output	DIO Port C Input
15	DIO Control	DIO Control Read-back

Page 2 - FIFO Control (Enhanced Feature Page)		
Base +	***Write Function***	***Read Function***
12	Expanded FIFO Depth	Expanded FIFO Depth Read-back
13	-	-
14	-	-
15	-	-

Page 3 - Autocalibration Registers		
Base +	***Write Function***	***Read Function***
12	EEPROM/TrimDAC Data	EEPROM/TrimDAC Data Read-back
13	EEPROM/TrimDAC Address	EEPROM/TrimDAC Address Read-back
14	Calibration Control	Calibration Status
15	Advanced Feature Access	FPGA Revision Code

Page 4 - dsPIC Interface (Enhanced Feature Page)		
Base +	***Write Function***	***Read Function***
12	dsPIC Data	dsPIC Data
13	dsPIC Address	dsPIC Address Read-back
14	Auto-calibration Command	Auto-calibration Status
15	dsPIC Programming Control	dsPIC Programming Status

Page 5 - D/A Waveform Generator (Enhanced Feature Page)		
Base +	***Write Function***	***Read Function***
12	Waveform Buffer Address (LSB)	-
13	Waveform Buffer Address (MSB)	-
14	Waveform Generator Control	Waveform Generator Control Read-back
15	Waveform Generator Command	-

Note: Page 6, CPLD I/O Window (Enhanced Feature Page), is a window to the CPLD I/O. This page should not be accessed in normal operation.

I/O Register Summary

Write Register Definitions

Base +	7	6	5	4	3	2	1	0
Main Register Set								
0	ADSTART							
1	-	-	-	-	LED	DOUT2	DOUT1	DOUT0
2	-	-	-	L4	L3	L2	L1	L0
3	-	-	-	H4	H3	H2	H1	H0
4	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
5	DACH1	DACH0	DASIM	DAGEN	DA11	DA10	DA9	DA8
6	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1
7	-	-	-	-	FIFOEN	SCANEN	FIFORST	-
8	-	-	RESETA	RESETD	INTRST	P2	P1	P0
9	ADINTE	DINTE	TINTE	RSVD1	DMAEN	-	CLKEN	CLKSEL
10	FREQ12	FREQ0	OUT2EN	OUT0EN	RSVD	GT0EN	SRC0	GT12EN
11	-	-	SCINT1	SCINT0	RANGE	ADBU	G1	G0
Page 0 - 82C54 Counter/Timer Access								
12	CTR0D7	CTR0D6	CTR0D5	CTR0D4	CTR0D3	CTR0D2	CTR0D1	CTR0D0
13	CTR1D7	CTR1D6	CTR1D5	CTR1D4	CTR1D3	CTR1D2	CTR1D1	CTR1D0
14	CTR2D7	CTR2D6	CTR2D5	CTR2D4	CTR2D3	CTR2D2	CTR2D1	CTR2D0
15	SC1	SC0	RW1	RW0	M2	M1	M0	BCD
Page 1 - 82C55-Type Digital I/O								
12	A7	A6	A5	A4	A3	A2	A1	A0
13	B7	B6	B5	B4	B3	B2	B1	B0
14	C7	C6	C5	C4	C3	C2	C1	C0
15	1	MODEC	MODEA	DIRA	DIRCH	MODEB	DIRB	DIRCL
Page 2 - FIFO Control (Enhanced Feature Page)								
12	-	-	-	-	-	-	-	FD9
13								
14								
15								
Page 3 - Autocalibration Registers								
12	D7	D6	D5	D4	D3	D2	D1	D0
13	-	A6	A5	A4	A3	A2	A1	A0
14	EE_EN	EE_RW	RUNCAL	MUXEN	TDACEN	-	-	-
15	EE_ACC							
Page 4 - dsPIC Interface (Enhanced Feature Page)								
12	PICD7	PICD6	PICD5	PICD4	PICD3	PICD2	PICD1	PICD0
13	PICR/W	-	-	PICA4	PICA3	PICA2	PICA1	PICA0
14	-	-	-	ACHOLD	ACREL	PICRST	ACABT	ACTRIB
15	PSTART	PSTOP	PGDOUT	PGDIN	PGDW1	PGDW0	PGCW1	PGCW0
Page 5 - D/A Waveform Generator (Enhanced Feature Page)								
12	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0
13	-	-	-	-	-	-	DACA9	DACA8
14	DEPTH3	DEPTH2	DEPTH1	DEPTH0	WGCH1	WGCH0	WGSRC1	WGSRC0
15	-	-	-	-	WGINC	WGRST	WGPS	WGSTRT

Read Register Definitions

Base +	7	6	5	4	3	2	1	0
Main Register Set								
0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
2	-	-	-	L4	L3	L2	L1	L0
3	-	-	-	H4	H3	H2	H1	H0
4	DACBUSY	CALBUSY	ACACT	-	DIN3	DIN2	DIN1	DIN0
5	-	-	-	-	-	-	-	FD9
6	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1
7	EF	TF	FF	OVF	FIFOEN	SCANEN	PAGE1	PAGE0
8	STS	S/D1	S/D0	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
9	ADINT	DINT	TINT	-	DMAEN	P2	CLKEN	CLKSEL
10	FREQ12	FREQ0	OUT2EN	OUT0EN	RSVD	GT0EN	SRC0	GT12EN
11	WAIT	RSVD	SCINT1	SCINT0	RANGE	ADBU	G1	G0
Page 0 - 82C54 Counter/Timer Access								
12	CTR0D7	CTR0D6	CTR0D5	CTR0D4	CTR0D3	CTR0D2	CTR0D1	CTR0D0
13	CTR1D7	CTR1D6	CTR1D5	CTR1D4	CTR1D3	CTR1D2	CTR1D1	CTR1D0
14	CTR2D7	CTR2D6	CTR2D5	CTR2D4	CTR2D3	CTR2D2	CTR2D1	CTR2D0
15	SC1	SC0	RW1	RW0	M2	M1	M0	BCD
Page 1 - 82C55-Type Digital I/O								
12	A7	A6	A5	A4	A3	A2	A1	A0
13	B7	B6	B5	B4	B3	B2	B1	B0
14	C7	C6	C5	C4	C3	C2	C1	C0
15	1	MODEC	MODEA	DIRA	DIRCH	MODEB	DIRB	DIRCL
Page 2 - FIFO Control (Enhanced Feature Page)								
12	-	-	-	-	-	-	-	FD9
13								
14								
15								
Page 3 - Autocalibration Registers								
12	D7	D6	D5	D4	D3	D2	D1	D0
13	-	A6	A5	A4	A3	A2	A1	A0
14	0	TDBUSY	EEBUSY	CMUXEN	TDACEN	0	0	0
15	REV							
Page 4 - dsPIC Interface (Enhanced Feature Page)								
12	PICD7	PICD6	PICD5	PICD4	PICD3	PICD2	PICD1	PICD0
13	I2CBUSY	-	-	PICA4	PICA3	PICA2	PICA1	PICA0
14	-	-	-	ACHOLD	PICPRST	ACERR	ACACT	PICBSY
15	-	-	-	-	-	-	-	PGDR
Page 5 - D/A Waveform Generator (Enhanced Feature Page)								
12	-	-	-	-	-	-	-	-
13	-	-	-	-	-	-	-	-
14	DEPTH3	DEPTH2	DEPTH1	DEPTH0	WGCH1	WGCH0	WGSRC1	WGSRC0
15	-	-	-	-	-	-	-	-

I/O Register Definitions

Note: In the register descriptions, below, writes to an undefined bit have no effect. Reads of an undefined bit return the value zero.

Main Register Set Definitions

Start A/D Conversion: Base+0 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	ADSTART							

ADSTART Writing any value to this register starts an A/D conversion, unless a conversion is already in progress (AD_BUSY high). An A/D conversion starts even if the board is set up for interrupt, DMA or external trigger mode.

A/D LSB (bits 7-0): Base+0 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

AD7-AD0 A/D data bits 7 - 0; AD0 is the LSB.

Auxiliary Digital Output: Base+1 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	LED	DOUT2	DOUT1	DOUT0

LED Toggles the on-board user LED; 1 = on, 0 = off.

DOUT2-0 Auxiliary digital output bits on analog I/O header CN12. Two pins also serve as optional counter outputs based on control register bits at Base+10:
DOUT2 - CN12, pin 28. Counter 2 output when OUT2EN = 1 (Base+10, bit 5).
DOUT1 - CN12, pin 30.
DOUT0 - CN12, pin 27. Counter 0 output when OUT0EN = 1 (Base+10, bit 4).

A/D MSB (bits 15-8): Base+1 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD15-8 A/D data bits 15 - 8; AD15 is the MSB.

A/D Low Channel: Base+2 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	L4	L3	L2	L1	L0

L4-L0 The low channel number setting in the A/D channel scan range. Channel numbers range from 0 to 31 in single-ended mode. Writing to this register updates the current channel internal register.

A/D high Channel: Base+3 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	H4	H3	H2	H1	H0

H4-H0 The high channel number setting in the A/D channel scan range. Channel numbers range from 0 to 31 in single-ended mode.

DAC LSB: Base+4 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

DA7-DA0 D/A data bits 7 - 0 for the channel currently being accessed. This register is a holding register. Writing to it does not affect any D/A channel until the MSB is written. When the MSB is written (see below, Base+5), the value written to that register, along with the value written to this register, are simultaneously written to the D/A chip's load register for the selected channel. See Base+5, write for more details.

Status/Auxiliary Digital Inputs: Base+4 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	DACBUSY	CALBUSY	ACACT	-	DIN3	DIN2	DIN1	DIN0

DACBUSY The D/A serial transfer is in progress. Do not attempt to write to the D/A converters at Base + 4 or Base + 5 while this bit is high. This bit must be checked before any write to these registers.

CALBUSY Calibration is in progress or EEPROM is being accessed. Do not attempt calibration or EEPROM access while this bit is high. This bit must be checked before any calibration or EEPROM operation is attempted.

ACACT This is a copy of the value found at Page 4, Base+14, bit 1. It is mirrored at this location to provide a page-independent means of seeing the AC status, since AC uses Page 3.

DIN3-DIN0 Auxiliary digital inputs on analog I/O header J3. These pins have multiple functions based on control bits at Base + 9 and Base + 10:

DIN3 - CN12, pin 31. External A/D clock when CLKSEL = 1 (Base + 9 bit 0)

DIN2 - CN12, pin 32. Gate for counters 1 and 2 when GT12EN = 1 (Base + 10 bit 0)

DIN1 - CN12, pin 26. Gate for counter 0 when GT0EN = 1 (Base + 10 bit 2)

DIN0 - CN12, pin 25. Clock for counter 0 when SRC0 = 1 (Base + 10 bit1)

DAC MSB + Channel: Base+5 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	DACH1	DACH0	DASIM	DAGEN	DA11	DA10	DA9	DA8

DACH1-0 Binary number of the D/A channel, 3 – 0.

DASIM D/A simultaneous update.

NOTE: If enhanced features are disabled this is always ‘0’ for backwards compatibility, meaning that D/A outputs will update on every write to this register.

1 = Latches D/A channel and output. Output will not change until this register is written to again with DASIM set to 0.

0 = Perform D/A simultaneous update. All previously latched D/A channels and and current channel will update.

DAGEN D/A wave form generator enable

NOTE: If enhanced features are disabled this is always ‘0’.

1 = Data is transferred to the D/A wave form memory block instead of the DAC chip. Used in conjunction with D/A wave form generator to store DAC code.

0 = Data is transferred to the DAC chip for output.

DA11-8 D/A bits 11 - 8 for the selected output channel; DA11 is the MSB

FIFO Threshold Read-back (bit 8): Base+5 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	FD9

FD9 FIFO threshold (bit 9). (See FIFO Threshold: Base+6, below)

FIFO Threshold: Base+6 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	FD8	FD7	FD6	FD5	FD4	FD3	FD2	FD1

FD8-FD1 FIFO threshold (bits 1-8). This is the level at which the board will generate an interrupt request when the FIFO is enabled (FIFOEN = 1 in Base + 7). Note that the value written is shifted by 1 bit, i.e. divided by 2. For example, if you want a FIFO threshold of 256 samples, write a 128 to this register.

The interrupt routine must read exactly this number of samples out each time it runs. The last time the routine runs, it should read whatever is remaining in the FIFO by monitoring the EF bit (Empty Flag) in the FIFO status register at Base + 7. When the FIFO is empty, EF = 1, and the FIFO returns the value hex FF on all read operations.

If you are sampling at a slow rate or want to control when the interrupt occurs, you can set the threshold to a low value. For example, if you are sampling 16 channels at 10Hz and you want an interrupt each set of samples, you can set the threshold to 16 (write an 8 to this register), so that an interrupt will occur each 16 samples. Then the interrupt routine should read out 16 samples from the FIFO, and you get new data as soon as it is available.

For higher sample rates (100KHz or higher) it may be necessary to increase the threshold above 256, to around 350 or even 512 with enhanced features enabled. If you set the threshold too high, you may overrun the FIFO, since the interrupt routine may not respond before the remaining locations are filled, causing an overflow. An overflow can be detected by checking the OVF bit in the FIFO status register at Base + 7. The correct threshold for your application can only be determined by testing.

FIFO Control: Base+7 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	FIFOEN	SCANEN	FIFORST	-

FIFOEN FIFO enable:
1 = Enable FIFO operation; if interrupts are enabled, interrupts will occur when the FIFO hits threshold (TF = 1). This slows down the interrupt rate dramatically compared to the actual A/D sample rate.
0 = Disable FIFO operation; if interrupts are enabled, interrupts will occur after each A/D conversion.

SCANEN Scan enable:
1 = Scan mode enabled; FIFO will fill up with data for a single scan, and STS will stay high until entire scan is complete; if interrupts are enabled, interrupts will occur on integral multiples of scans.
0 = Scan mode disabled; The STS bit will correspond directly to the status indicator from the A/D converter.

FIFORST FIFO reset:
1 = Reset FIFO; after this command is issued, EF = 1, TF = 0, FF = 0.
0 = No function.

FIFO Status: Base+7 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	EF	TF	FF	OVF	FIFOEN	SCANEN	PAGE1	PAGE0

EF Empty flag:
1 = FIFO is empty.
0 = FIFO is not empty.

TF Threshold flag:
1 = FIFO is at or beyond threshold; if the FIFO threshold is 256 words, this flag is set when the FIFO contains at least 256 words of A/D data.
0 = FIFO is less than threshold.

FF Full flag:
1 = FIFO is full; the next A/D conversion will result in an overflow.
0 = FIFO is less than full.

OVF Overflow flag:
1 = FIFO has overflowed; data has been lost. This flag is cleared on the next successful A/D read.
0 = FIFO has not overflowed since the last A/D data read.

FIFOEN FIFO enable read-back.

SCANEN Scan enable read-back.

PAGE0-1 Read-back of the current page register setting. (See Base+8 below)

Miscellaneous and Page Control: Base+8 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	RESETA	RESETD	INTRST	P2	P1	P0

RESETA Writing a 1 to this bit causes a full reset of all features of the board, including the DACs, the FIFO, the digital I/O, and all internal registers. The counter/timers are not affected by this reset.

RESETD Writing a 1 to this bit causes a reset identical to above except the analog outputs are not affected.

INTRST Writing a 1 to this bit resets the interrupt request circuit on the board. The programmer must write a 1 to this bit during the interrupt service routine, or further interrupts will not occur. Writing a 1 to this bit does not disturb the values of the PAGE bits.

P2-P0 Three-bit value that selects which I/O device is accessible through the registers at locations Base + 12 through Base+15:

P<2:0>	***Page***	***Device***
000	0	8254
001	1	8255
010	2	FIFO Control
011	3	EEPROM/TrimDAC
100	4	dsPIC
101	5	D/A Waveform Generator
110	6	Factory Use Only
111	7	Not Used

Grayed pages (2, 4, 5, 6 and 7) are only accessible when the enhanced features are enabled. Note that P2 is an enhanced feature bit.

Writing to the page bits will not generate a board reset or interrupt reset, as long as those bits are kept at 0 in the data written to this register.

A/D Status: Base+8 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	STS	S/D1	S/D0	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0

STS A/D chip status:
1 = A/D conversion or A/D scan in progress.
0 = A/D idle.

S/D1-0 Single-ended / Differential A/D input mode indicator. S/D1 controls the channels 8-15 and 24-31, S/D0 controls 0-7 and 16-23.
1 = Single-ended (default).
0 = Differential.

ADCH4-0 Current A/D channel; this is the channel currently selected on board and is the channel that will be used for the next A/D conversion (unless a new value is written to the low channel register).

Interrupt and A/D Clock Control: Base+9 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	ADINTE	DINTE	TINTE	RSVD1	DMAEN	-	CLKEN	CLKSEL

ADINTE A/D interrupt enable:
1 = Enable A/D interrupt operation.
0 = Disable A/D interrupt operation.

DINTE Digital interrupt enable:
1 = Enable digital I/O interrupt operation.
0 = Disable digital I/O interrupt operation.

TINTE Timer 0 interrupt enable:
1 = Enable counter/timer 0 interrupt operation.
0 = Disable counter/timer 0 interrupt operation.

RSVD1 Reserved for future use

DMAEN DMA Enable. This bit is ignored if enhanced features are disabled. See DMA signal definition for more detail on DMA behavior.
1 = DMA Enabled.
0 = DMA Disabled.

CLKEN Enable hardware clock for A/D sampling:
1 = Enable hardware clock for A/D (source is selected with CLKSEL bit below);
NOTE: When this bit is 1, software triggers are disabled, i.e. writing to Base + 0 will not start an A/D conversion.
0 = Disable hardware clocking for A/D; A/D conversions occur with software command only.

CLKSEL Hardware clock select (enabled only when CLKEN = 1 above):
1 = Internal clock: Falling edges on the output of counter/timer 2 generate A/D conversions. Counter 2 is in turn driven by counter 1, which is driven by the clock selected by bit FREQ12 in Base + 10 below.
0 = External trigger: Falling edges on the DIN3/EXTCLK pin on the I/O header generate A/D conversions.

Interrupt and A/D Clock Status: Base+9 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	ADINT	DINT	TINT	-	DMAEN	P2	CLKEN	CLKSEL

ADINT A/D interrupt status; Cleared by writing to INTRST (Base+8).
1 = A/D interrupt request has occurred.
0 = No interrupt request.

DINT Digital interrupt status; Cleared by writing to INTRST (Base+8).
1 = Digital interrupt request has occurred.
0 = No interrupt request.

TINT Timer interrupt status; Cleared by writing to INTRST (Base+8).
1 = Timer interrupt request has occurred.
0 = No interrupt request.

DMAEN Read-back of control register bit defined, above.

P2 Read-back of P2 register bit defined at Base+8/write.

CLKEN Read-back of control register bit defined, above.

CLKSEL Read-back of control register bit defined, above.

Counter/Timer and DIO Control: Base+10 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	FREQ12	FREQ0	OUT2EN	OUT0EN	RSVD	GT0EN	SRC0	GT12EN

FREQ12 Input frequency select for the counter 1-2 cascade:

1 = Input to counter 1 is a 100KHz (one hundred, not ten) frequency derived from the on-board 10MHz oscillator.

0 = Input to counter 1 is 10MHz from the on-board oscillator.

FREQ0 Input frequency select for counter 0 when SRC0 = 1 (bit 1):

1 = Input to counter 0 is a 10KHz (ten, not one hundred) frequency derived from the on-board 10MHz oscillator.

0 = Input to counter 0 is 10MHz from the on-board oscillator.

OUT2EN Counter/timer 2 output enable:

1 = Counter 2 output appears on I/O header CN12, pin 28.

0 = CN12, pin 28, is controlled by bit DOUT0 at Base+1.

OUT0EN Counter/timer 0 output enable:

1 = Counter 0 output appears on I/O header CN12 pin 27, OUT 0 / DOUT 0.

0 =.OUT 0 / DOUT 0 pin is set by bit DOUT0 at Base+1.

RSVD Reserved for future use

GT0EN Counter/timer 0 gate enable:

1 = Gate 0 / DIN 1, CN12 pin 26, acts as an active high gate for counter/timer 0. This pin is connected to a 10KΩ pull-up resistor.

0 = Counter/timer 0 runs freely with no gating.

SRC0 Counter 0 input source:

1 = Input to Counter 0 is the clock determined by FREQ0 (bit 6).

0 = Input to Counter 0 is CN12 pin 25 (CLK 0 / DIN 0). The falling edge is active. This pin is connected to a 10KΩ pull-up resistor.

GT12EN Counter/timer 1/2 and external trigger gate enable:

This bit enables gating for A/D sampling for both internal and external clocking.

1 = When CN12 pin 32 (EXTGATE / DIN 2) is low prior to the start of A/D conversions, A/D conversions will not begin until it is brought high (trigger mode).

If the pin is brought low while conversions are occurring, conversions will pause until it is brought high (gate mode). CN12 pin 32 is connected to a 10KΩ pull-up resistor.

0 = The interrupt operation begins immediately once it is set up and the selected clock source begins, with no external triggering or gating.

Analog Configuration: Base+11 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	SCINT1	SCINT0	RANGE	ADBU	G1	G0

SCINT1-0 Scan interval. This is the time between A/D samples when performing a scan (SCANEN = 1). The driver sets a default of 10µs.

SCINT1	*SCINT0*	*Interval*
0	0	20uS
0	1	15uS
1	0	10uS
1	1	4uS

RANGE 5V or 10V A/D positive full-scale voltage (0 = 5V, 1 = 10V)

ADBU A/D bipolar/unipolar setting; 0 = bipolar, 1 = unipolar. These control bits define the A/D input range for a gain setting of 1.

RANGE	*ADBU*	*A/D Range*
0	0	+/- 5V
0	1	0-5V
1	0	+/- 10V
1	1	0-10V

G1-0 A/D programmable gain amplifier setting:

G1	*G0*	*Gain*
0	0	1
0	1	2
1	0	4
1	1	8

The gain setting is the ratio between the full-scale voltage range at the A/D converter and the full-scale voltage range at the input to the board. The gain should never cause the input signal to exceed the range of the A/D, because incorrect measurements will result (clipping).

The A/D full-scale voltage range is defined by the RANGE and ADBU bits above. To calculate the optimum gain setting, select the highest gain that does not allow the input signal to exceed the selected A/D range over its entire expected fluctuation range. Note that these settings can be changed at any time, even between A/D conversions, so you can tune the board's settings to each input signal.

Note: On power up or system reset, the board is configured for A/D bipolar mode, input range = ±5V, and gain = 1, corresponding to all zeros in this register.

Analog I/O Read-back: Base+11 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	WAIT	RSVD	SCINT1	SCINT0	RANGE	ADBU	G1	G0

WAIT Analog input circuit settling time holdoff indicator:

1 The analog input circuit is settling on a new signal and is not yet ready for a new conversion to start; this will occur each time you change the channel, gain, or input range on the board. The wait time is approximately 10µS.

0 The analog input circuit has settled, and a new A/D conversion may begin.

RSVD Reserved for future use.

SCINT1-0 Read-back of control bit described, above. Only available if enhanced features are enabled.

RANGE Read-back of control bit described, above.

ADBU Read-back of control bit described, above.

G1-0 Read-back of control bit described, above.

Page 0 Register Definitions

This section is included as a reference to the page 0 counter/timer registers. Behavior of these registers should be identical to the 82C54 counter/timer chip. Please, read the 82C54 datasheet, for this behavior.

Counter 0 Data: Base+12 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	CTR0D7	CTR0D6	CTR0D5	CTR0D4	CTR0D3	CTR0D2	CTR0D1	CTR0D0

CRT0D7-0 Counter 0 data.

Counter 1 Data: Base+13 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	CTR1D7	CTR1D6	CTR1D5	CTR1D4	CTR1D3	CTR1D2	CTR1D1	CTR1D0

CRT1D7-0 Counter 1 data.

Counter 2 Data: Base+14 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	CTR2D7	CTR2D6	CTR2D5	CTR2D4	CTR2D3	CTR2D2	CTR2D1	CTR2D0

CRT2D7-0 Counter 2 data.

82C54 Control: Base+15 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC1-0 Counter select.

RW1-0 Read/write mode.

M2-0 Timer mode.

BCD Binary Coded Decimal counter.

Page 1 Register Definitions

This section is included as a reference to the page 1 82C55-like digital I/O registers.

DIO Port A I/O: Base+12 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	A7	A6	A5	A4	A3	A2	A1	A0

A7-A0 Port A data.

DIO Port B I/O: Base+13 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	B7	B6	B5	B4	B3	B2	B1	B0

B7-B0 Port B data.

DIO Port C I/O: Base+14 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	C7	C6	C5	C4	C3	C2	C1	C0

C7-C0 Port C data.

DIO Control: Base+15 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	1	MODEC	MODEA	DIRA	DIRCH	MODEB	DIRB	DIRCL

MODEC-A Mode configuration bits. These must be set to 0.

DIRA
DIRCH
DIRB
DIRCL

Direction control bits. On ports A and B, all the bits in each port must be the same direction. On port C, the upper half C7–C4 can have a different direction than the lower half C3–C0.
0 = Output.
1 = Input.

Note: Bit 7 must be set to 1. This indicates port configure mode in the 8255 (as opposed to bit set mode, which is not supported).

Page 2 Register Definitions

This is an enhanced features page. It is only accessible when enhanced features are enabled.

Expanded FIFO Depth: Base+12 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	FD9

FD9 This bit is used when setting the FIFO threshold. See the documentation for register Base+6 for more information.

Page 3 Register Definitions

These registers are used to control the auto-calibration process. For user software-controlled auto-calibration, these registers are used by the Universal Driver software or the user's software to manage the calibration process. For auto-auto-calibration, the on-board dsPIC microcontroller uses these registers to manage the auto-calibration automatically.

EEPROM/TrimDAC Data: Base+12 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	D7	D6	D5	D4	D3	D2	D1	D0

D7-D0 Calibration data to be read or written to the EEPROM and/or TrimDAC.
During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.
During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after EEBUSY = 0.
The TrimDAC data cannot be read back.

EEPROM/TrimDAC Address: Base+13 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	A6	A5	A4	A3	A2	A1	A0

A6-A0 EEPROM/TrimDAC address.
The EEPROM recognizes address 0 – 127 using address bits A6 – A0 of this register. The TrimDAC only recognizes addresses 0 – 7 using bits A2 – A0. In each case, remaining address bits will be ignored.

Calibration Control: Base+14 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	EE_EN	EE_RW	RUNCAL	MUXEN	TDACEN	-	-	-

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit.

EE_RW Selects read or write operation for the EEPROM: 0 = Write, 1 = Read.

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM.

MUXEN Calibration multiplexor enable. The cal mux is used to read precision on-board reference voltages that are used in the autocalibration process. It also can be used to read back the value of analog output 0.
1 enable cal mux and disable user analog input channels.
0 disable cal mux, enable user inputs.

TDACEN TrimDAC Enable. Writing 1 to this bit initiates a transfer to the TrimDAC (used in the autocalibration process).

Calibration Status: Base+14 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	0	TDBUSY	EEBUSY	CMUXEN	TDACEN	0	0	0

TDBUSY TrimDAC busy indicator:
0 = User may access TrimDAC.
1 = TrimDAC is being accessed; user must wait.

EEBUSY EEPROM busy indicator:
0 = User may access EEPROM.
1 = EEPROM is being accessed; user must wait.

CMUXEN Calmux enable status:
0 = Calibration multiplexor is not currently enabled.
1 = Calibration multiplexor is enabled and may be updated.

TDACEN TrimDAC enable status:
0 = TrimDAC is not enabled.
1 = TrimDAC is enabled and may be updated.

Advanced Feature Access: Base+15 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	EE_ACC							

EE_ACC EEPROM access. After entering page 3 by setting the Page bits, the user must write the value 0xA5 (binary 10100101) to this register in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents. Once the page is set and this value is written, you can make unlimited reads and writes to the EEPROM without resending this key as long as you stay on page 3.

Writing 0xA6 to this register enables all enhanced features and sets A/D FIFO depth to 1024 samples. This enhanced feature state remains in effect until explicitly disabled.

Writing 0xA7 to this register disables all enhanced features. This is the default power-on state. Writing 0xA7 to this register automatically halts any enhanced feature currently running, internally clears all enhanced registers to their default state, and resets the A/D FIFO depth to 512.

FPGA Revision Code: Base+15 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	REV							

REV This register is the revision level of the FPGA design. This value changes with new versions of the FPGA. It provides a way to distinguish between different versions of FPGA code.

Page 4 Register Definitions

This is an enhanced features page. It is only accessible when enhanced features are enabled.

dsPIC Data: Base+12 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	PICD7	PICD6	PICD5	PICD4	PICD3	PICD2	PICD1	PICD0

PICD7-0 Data to read/write to/from the PIC microcontroller. The data must be written to this register before the address and read/write bit is written to Base+13, below.

dsPIC Address: Base+13 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	PICR/W	-	-	PICA4	PICA3	PICA2	PICA1	PICA0

PICR/W Read/write control: 0 = write, 1 = read.

PICA4-0 dsPIC internal address.
Writing a byte with R/W = 0 causes the dsPIC to write the data contained in the dsPIC Data Register, above, to the dsPIC internal address indicated by PICA4-0.
Writing a byte with R/W = 1 causes the dsPIC to read the data at dsPIC internal address, PICA4-0, and places the received data in the dsPIC Data Register.

dsPIC Address Read-back: Base+13 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	I2CBUSY	-	-	PICA4	PICA3	PICA2	PICA1	PICA0

I2CBUSY I2C port status bit:
0 = Last I2C operation completed.
1 = Last I2C operation in progress.

PICA4-0 dsPIC address last accessed.

Auto-calibration Command: Base+14 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	ACHOLD	ACREL	PICRST	ACABT	ACTRIB

ACHOLD Auto-autocal process is disabled. Autocalibration must be triggered by software.

ACREL Auto-autocal process is enabled. Auto-autocalibration will occur whenever the board requires it.

PICRST Reset dsPIC device. This command is normally not needed.

ACABT Abort any currently running auto-autocal operation immediately.

ACTRIB Initiate an auto-autocal process immediately.

Note: Set the desired bit to a value of 1 to execute the desired command. Only one bit can be set to 1 at a time. Bits are processed MSB to LSB. The first 1 bit determines which command is executed.

Auto-calibration Status: Base+14 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	ACHOLD	PICPRST	ACERR	ACACT	PICBSY

ACHOLD 1 = dsPIC in holdoff mode (auto-autocal disabled).

PICPRST 1 = dsPIC device present on board.

ACERR 1 = dsPIC detected errors during last Auto-autocal process

ACACT 1 = Auto-autocal process currently in progress..

PICBSY 1 = dsPIC busy, either with auto-autocal or some other activity.

dsPIC Programming Control: Base+15 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	PSTART	PSTOP	PGDOUT	PGDIN	PGDW1	PGDW0	PGCW1	PGCW0

PSTART Drive EN_PROG# signal low.

PSTOP Drive EN_PROG# high.

PGDOUT FPGA makes PIC_PGD line an output, but leave at current level (i.e. perform input to find current level, set line as an output at same level).

PGDIN FPGA makes PIC_PGD line an input..

PGDW1 If PIC_PGD line is in output mode, set high.

PGDW0 If PIC_PGD line is in output mode, set low.

PGCW1 Set PIC_PGC line high.

PGCW0 Set PIC_PGC line low.

Note: This register is used to control the on-board dsPIC microcontroller. The dsPIC controls the auto-autocalibration process, and it also provides the communication link between the board and its serial port. Only one bit can be set to 1 at a time. Bits are processed MSB to LSB. The first 1 bit determines which command is executed.

dsPIC Programming Status: Base+15 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	-	PGDR

PGDR Reads back current level of PIC_PGD line (low = 0, high = 1).

Page 5 Register Definitions

This is an enhanced features page. It is only accessible when enhanced features are enabled.

Waveform Buffer Address (LSB): Base+12 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	DACA7	DACA6	DACA5	DACA4	DACA3	DACA2	DACA1	DACA0

DACA7-0 LSB of address to store D/A code in D/A waveform buffer.

Waveform Buffer Address (MSB): Base+13 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	-	-	DACA9	DACA8

DACA9-8 MSB of address to store D/A code in D/A waveform buffer.

Waveform Generator Control: Base+14 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	DEPTH3	DEPTH2	DEPTH1	DEPTH0	WGCH1	WGCH0	WGSRC1	WGSRC0

DEPTH3-0 These bits define the size of the D/A waveform buffer. The depth is based on this equation:

Depth = [(DEPTH3-0) + 1] * 64

This allows valid depth values from 64 to 1024 samples.

The waveform generator frame pointer will return to 0 whenever it hits either 1024 or the depth value indicated above.

WGCH1-0 These two bits combine to choose how many codes are output on each frame.

WGCH1	***WGCH0***	***Description***
0	0	One code per frame
0	1	Two codes per frame
1	X	Four codes per frame

WGSRC1-0 These two bits combine to choose which trigger source is used to increment the waveform by one frame.

WGSRC1	***WGSRC0***	***Description***
0	0	Manual (using WGINC)
0	1	Counter 0 output
1	0	Counter 1/2 output
1	1	External trigger (CN12, pin 31)

Waveform Generator Command: Base+15 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	-	WGINC	WGRST	WGPS	WGSTRT

WGINC Begin or resume the waveform generator.

WGRST Pause/stop the waveform generator. The current position in memory is saved for the next begin/resume, or can be reset using WGRST.

WGPS Reset the waveform generator to output from the beginning of the D/A code buffer.

WGSTRT Force the waveform generator to increment one frame.

Note: Only one bit can be set to 1 at a time. Bits are processed MSB to LSB. The first 1 bit determines which command is executed.

Enabling Enhanced Features

Poseidon has many newly added features that are only accessible when "enhanced features" is enabled. These features include D/A wave form generator (access to Page 5), larger FIFO size of 1024 (access to Page 2), dsPIC and auto autocalibration (access to Page 4), and various others.

Enhanced Mode

Two steps are required to enable enhanced features.

1. Set page bits to Page 3.
2. Write code to unlock enhanced features.

Below is the code demonstrating how to enable enhanced features without using the driver software. The page bit can be set using the register at Base+8.

```
outp(Base + 8, 0x3);
```

Write 0xA6 to register Base+15 to unlock enhanced features.

```
outp(Base + 15, 0xA6);
```

Normal Mode

To disable enhanced features follow the same instructions as above except write 0xA7 instead of 0xA6 to register Base+15.

```
outp(Base + 15, 0xA7);
```

Analog-to-Digital Input Ranges and Resolution

Overview

Poseidon uses a 16-bit A/D converter. This means that the analog input voltage can be measured to the precision of a 16-bit binary number. The maximum value of a 16-bit binary number is 216 - 1, or 65535, so the full range of numerical values that you can get from a Poseidon analog input channel is 0 - 65535.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of one in the A/D code, and is referred to as one Least Significant Bit (1 LSB).

Unipolar and Bipolar Inputs

Poseidon can measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. The full-scale input voltage range depends on the Gain, Range, and Polarity bit settings in the Analog Configuration Register at Base+11. In front of the A/D converter is a programmable gain amplifier that multiplies the input signal before it reaches the A/D. This gain circuit has the effect of scaling the input voltage range to match the A/D converter for better resolution. In general, you should select the highest gain you can that will allow the A/D converter to read the full range of voltages over which your input signals will vary. If the gain is too high, the A/D converter will clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

Input Ranges and Resolutions

The table below lists the full-scale input range for each valid analog input configuration. The parameters Polarity, Range and Gain are combined to create the value "Code", which is the value that you must write to the analog configuration register at Base+11 to get the input range shown. A total of nine different input ranges are possible. Note that the range programming codes 4, 5, 6 and 7 are invalid and that range codes 9 – 11 are equivalent to range codes 0 – 2.

Polarity	*Range*	*Gain*	*Code*	*Input Range*	*Resolution (1 LSB)*
Bipolar	5V	1	0	± 5V	153µV
Bipolar	5V	2	1	± 2.5V	76µV
Bipolar	5V	4	2	± 1.25V	38µV
Bipolar	5V	8	3	± 0.625V	19µV
Unipolar	5V	1	4	Invalid Setting	
Unipolar	5V	2	5	Invalid Setting	
Unipolar	5V	4	6	Invalid Setting	
Unipolar	5V	8	7	Invalid Setting	
Bipolar	10V	1	8	± 10V	305µV
Bipolar	10V	2	9	± 5V	153µV
Bipolar	10V	4	10	± 2.5V	76µV
Bipolar	10V	8	11	± 1.25V	38µV
Unipolar	10V	1	12	0-10V	153µV
Unipolar	10V	2	13	0-5V	76µV
Unipolar	10V	4	14	0-2.5V	38µV
Unipolar	10V	8	15	0-1.25V	19µV

A/D Conversion Formulas

The 16-bit value returned by the A/D converter is always a twos complement number ranging from -32768 to 32767, regardless of the input range. This is because the input range of the A/D is fixed at ±10V. The input signal is actually magnified and shifted to match this range before it reaches the A/D. For example, for an input range of 0-10V, the signal is first shifted down by 5V to ±5V and then amplified by two to become ±10V.

Therefore, two different formulas are needed to convert the A/D value back to a voltage, one for bipolar ranges, and one for unipolar ranges.

To convert the A/D value to the corresponding input voltage, use the following formulas.

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D code / 32768 * Full-scale input range

Example:

Given, Input range is ±5V and A/D code is 17761.

Therefore,

Input voltage = 17761 / 32768 * 5V = 2.710V.

For a bipolar input range,

1 LSB = 1/32768 * Full-scale voltage.

The table, below, shows the relationship between A/D code and input voltage for a bipolar input range (VFS = Full scale input voltage).

A/D Code	***Input Voltage Symbolic Formula***	***Input Voltage for ±5V Range***
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
...	...	...
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
...	...	...
32767	V_{FS} - 1 LSB	4.9998V

Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D code + 32768) / 65536 * Full-scale input range

Example:

Given, Input range is 0-10V and A/D code is 17761.

Therefore,

Input voltage = (17761 + 32768) / 65536 * 10V = 7.7103V.

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

The following table illustrates the relationship between A/D code and input voltage for a unipolar input range (VFS = Full scale input voltage).

A/D Code	***Input Voltage Symbolic Formula***	***Input Voltage for 0–10V Range***
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.153mV
...	...	...
-1	V_{FS} / 2 - 1 LSB	4.99985V
0	V_{FS} / 2	5.0000V
1	V_{FS} / 2 + 1 LSB	5.00015V
...	...	...
32767	V_{FS} - 1 LSB	9.9998V

Performing an A/D Conversion

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (without the driver software).

All A/D conversions are stored in an on-board FIFO (first in first out memory). The FIFO can hold up to 1024 samples. Each time an A/D conversion is finished, the data is stored in the FIFO, and the FIFO counter increments by 1. Each time you read A/D data, you are actually reading it out of the FIFO, and the FIFO counter decrements by 1. When the FIFO is empty the data read from it is undefined; you may continue to read the last sample, or you may read all 1s.

You can read each A/D sample as soon as it is ready, or you can wait until you take a collection of samples (up to 1024 maximum) and then read them all out at once.

To be sure that you are getting only current A/D data, be sure to reset the FIFO each time before you start any A/D operation. This will prevent errors caused by leaving data in from a previous operation. To reset the FIFO, write a 1 to bit 2 of register Base+7. This bit is not a real register bit but triggers a command in the board's controller chip. Therefore, you do not need to write a 1 followed by a 0. However, writing to the FIFORST bit affects the values of other bits in this register as well:

```
outp(Base+7, 0x02); // resets the FIFO and clears SCANEN and FIFOEN
outp(Base+7, 0x0A); // resets the FIFO and SCANEN but leaves FIFOEN set
```

Note that this register also contains a FIFO enable bit, FIFOEN. This bit only has meaning during A/D interrupt operations. The FIFO is always enabled and is always in use during A/D conversions.

Perform an A/D conversion according to the following steps. Each step is discussed in detail, below.

1. Select the input channel.
2. Select the input range.
3. Wait for analog input circuit to settle.
4. Initiate an A/D conversion.
5. Wait for the conversion to finish.
6. Read the data from the board.
7. Convert the numerical data to a meaningful value.

If you are going to sample the same channel multiple times or sample multiple consecutive channels with the same input range, you only need to perform steps 1-3 once, and then you can repeat steps 4-6 or 4-7 as many times as desired.

Diamond Systems also provides sample register level code, downloadable at:

http://diamondsystems.com/files/binaries/SourceCodeExamples.zip

Select the Input Channel

Poseidon contains a channel counter circuit that controls which channel will be sampled on each A/D conversion command. The circuit uses two channel numbers called the low channel and high channel. These are stored in registers at Base+2 and Base+3. The circuit starts at the low channel and automatically increments after each A/D conversion until the high channel is reached. When an A/D conversion is performed on the high channel, the circuit

resets to the low channel and starts over again. This behavior enables you simplify your software by setting the channel range just once.

To read continuously from a single channel, write the same channel number to both the low channel and high channel registers.

To read from a series of consecutively numbered channels, write the starting channel to Base+2 and the ending channel to Base+3.

To read from a group of non-consecutive channels, you must treat each as a single channel, as described above.

Select the Input Range

Select the code corresponding to the desired input range and write it to the analog I/O control register at Base+11. You only need to write to this register if you want to select a different input range from the one used for the previous conversion. If all channels will be using the same input range, you can configure this register just once at the beginning of your procedure.

You can read the current value of this register by reading from Base+11.

Wait for Analog Input Circuit to Settle

After changing either the input channel or the input range, you must allow the circuit to settle on the new value before performing an A/D conversion. The settling time is long compared to software execution times, so a timer is provided on board to indicate when it is safe to proceed with A/D sampling. The WAIT bit at Base+11 indicates when the circuit is settling and when it is safe to sample the input. When WAIT is 1, the board is settling. When WAIT is 0, the board is ready for an A/D conversion.

Perform an A/D Conversion on the Current Channel

To generate an A/D conversion, simply write to Base+0 to start the conversion. Any value may be written to the register.

Wait for the Conversion to Finish

The A/D converter takes about four microseconds to complete a conversion. If you try to read the A/D converter data immediately after starting a conversion, you will get invalid data. Therefore, the A/D converter provides a status signal to indicate whether it is busy or idle. This signal can be read back as the STS bit in the status register at Base+8. When the A/D converter is busy (performing an A/D conversion) this bit is 1. When the A/D converter is idle (conversion is done and data is available) this bit is 0.

Read the Data from the Board

Once the conversion is complete, you can read the data back from the A/D converter. The data is 16 bits wide and is read back in two 8-bit bytes at Base+0 and Base+1. The low byte must be read first.

Note: Reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value with 8-bit accesses:

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

Alternatively, the value can be read as one 16-bit value, which is preferred since this method increases overall system bandwidth while reading data from the FIFO. For example,

```
Data = inpw(base); // Where the MSB and LSB are read in one access
```

The final data ranges from 0 to 65535 (0 to 256 - 1) as an unsigned integer. This value must be interpreted as a signed integer ranging from -32768 to +32767.

As noted above, all A/D conversions are stored in an on-board FIFO, which can hold up to 1024 samples in enhanced mode or 512 samples in normal mode. Whenever you read A/D data you are actually reading it out of the FIFO. Therefore, you can read each A/D sample as soon as it is ready, or you can wait until you take a collection of samples (up to 1024 maximum) and then read them all out in sequence.

Convert the numerical data to a meaningful value

Once you have the A/D value, you need to convert it to a meaningful value. The A/D conversion formulas describe how to convert the A/D data back to the original input voltage. You may also convert the result into engineering units. The two conversions can be done sequentially, or the formulas can be combined into a single formula.

A/D Sampling Methods

Sampling Modes

There are several different A/D sampling modes available on Poseidon. The mode in use is selected with the FIFO enable and Scan enable bits at the FIFO control register at Base+7 as well as the A/D interrupt enable bit in the Interrupt control register at Base+9.

> **Note: If interrupts are not enabled, the FIFO should not be enabled. FIFO storage is only useful when interrupts are used. Otherwise, the FIFO has no effect.**

All of these features may be selected as arguments to function calls in the driver software. The control register details are provided for completeness and for programmers not using the driver.

SCAN	*FIFO*	*Interrupt*	*Mode*	*Description*
No	No	No	Single Conversions	The most basic sampling method. Used for low-speed sampling (typically up to about 100Hz) under software control where a precise rate is not required, or under external control where the rate is slow. Consists of either one channel or multiple channels sampled one at a time.
Yes	No	No	Scan Conversions	Used to sample a group of consecutively numbered channels in rapid succession, under software or external control. The time between samples in a scan is programmable between 5 to 20 microseconds, while the time between scans depends on the software or external trigger and may be very short or very long, but is usually less than about 100Hz (above this rate use interrupt scans below).
No	No	Yes	Interrupt Single Conversion, Low Speed	Used for controlled-rate sampling of single channels or multiple channels in round-robin fashion, where the frequency of sampling must be precise but is relatively slow (less than 100Hz). The sampling clock comes from the on-board counter/timer or from an external signal. The interval between all A/D samples is identical.
Yes	No	Yes	Interrupt Scans, Low Speed	Used for controlled-rate sampling a group of channels in low-speed mode (less than 500Hz per channel). Each sampling event consists of a group of channels sampled in rapid succession. The time between scans is determined by the sample rate.
No	Yes	Yes	Interrupt Single Conversions, High Speed	Intended for medium- to high-speed operation (recommended above about 500Hz). Can support sampling rates up to the board's maximum of 250,000Hz. May also be used at slower rates if desired. The sampling clock comes from the on-board counter/timer or from an external signal.
Yes	Yes	Yes	Interrupt Scan Conversions	Used for high-speed sampling of a group of channels where the scan rate is high. The sampling clock comes from the on-board counter/timer or from an external signal.

FIFO Description

Poseidon uses a 1024-sample FIFO (First In First Out) memory buffer to manage A/D conversion data. It is used to store A/D data between the time it is generated by the A/D converter and the time it is read by the user program. In enhanced mode, the entire 1024-sample FIFO is available. In normal mode only 512 samples are available. The FIFO may be enabled and disabled under software control.

In single-conversion mode, the FIFO features are not generally needed so FIFO use should not be selected, although, the FIFO is still actually being used. Each A/D sample is stored in the FIFO. When the software reads the data, it reads it out of the FIFO. In low-speed sampling, each time a conversion occurs, the program reads the data, so there is always a one-to-one correspondence between sampling and reading. Thus, the FIFO contents never exceed one sample.

For high-speed sampling or interrupt operation, the FIFO substantially reduces the amount of software overhead in responding to A/D conversions as well as the interrupt rate on the bus because it enables the program to read multiple samples rather than one at a time. In addition, the FIFO is required for sampling rates in excess of the maximum interrupt rate possible on the bus. Generally, the fastest sustainable interrupt rate on the ISA bus running DOS is around 40,000 per second. Since Poseidon can sample up to 250,000 times per second, the FIFO is needed to reduce the interrupt rate at high speeds. When the interrupt routine runs, it reads multiple samples from the FIFO. The interrupt rate is equal to the sample rate divided by the number of samples read each interrupt. On Poseidon, this number is programmable using the register at Base+6. The usual value is 1/2 the maximum FIFO depth, or 512 samples. Therefore, the maximum interrupt rate for Poseidon is reduced to 488 per second, which easily sustainable on any popular operating system.

> **Note:: If both Scan and FIFO operation are enabled, the interrupt still occurs at the programmed FIFO threshold and the interrupt routine reads the indicated number or samples and then exits. This happens even if the number of samples is not an integral number of scans. For example, if you have a scan size of 10 and a FIFO threshold of 256, the first time the interrupt routine runs, it reads 256 samples, consisting of 25 full scans of all 10 channels followed by 6 samples from the next scan. The next time the interrupt routine runs, it reads the next 256 samples, consisting of the remaining 4 samples from the last scan it started to read, the next 25 full scans of 10 samples, and the first 2 samples of the next scan. This continues until the interrupt routine ends in either one-shot or recycle mode. In one-shot mode, the last time the interrupt routine runs it reads the entire contents of the FIFO, making all data available.**

Scan Sampling

A scan is defined as a quick burst of samples of multiple consecutive channels. For example, you may want to sample channels 0-15 all at once, and repeat the operation each second. This would be a scan at a frequency of 1Hz. Each time the A/D clock occurs (software command, timer, or external trigger), all 16 channels are sampled in high-speed succession. There is a short delay of 4 – 20 microseconds between each sample in the scan. Since each clock pulse causes all channels to be sampled, the effective sampling rate for each channel is the same as the programmed rate, and the total sampling rate is the programmed sampling rate times the number of channels in the scan range.

Scan sampling is independent of FIFO operation. Either or both can be enabled independently.

Sequential Sampling

In sequential sampling, each clock pulse results in a single A/D conversion on the current channel. If the channel range is set to a single channel (high channel = low channel), each conversion is performed on the same input channel. If the channel range is set to more than one channel (high channel > low channel), then the channel counter increments to the next channel in the range, and the next conversion is performed on that channel. When a conversion is performed on the high channel, the channel counter resets to the low channel for the next conversion. The intervals between all samples are equal. Since each clock pulse results in only one channel being sampled, the effective sampling rate is the programmed sampling rate divided by the number of channels in the channel range.

How To Perform Conversions Using Interrupts

Poseidon contains the ability to generate hardware interrupts to manage A/D conversions. Interrupt-based A/D conversions are used in several situations.

- High-speed sampling.
- Applications where the sampling rate must be precise.
- Applications where the sampling rate is based on an external clock.

The Diamond Systems Universal Driver functions *dscADSampleInt()* and *dscADSetSettings()* manage all of the required parameters to generate interrupt-based A/D conversions. Below is a checklist to help you configure the function call properly. All parameters are passed in the data structure of type *DSCAIOINT* for function *dscADSampleInt()* except for the input range.

1. A/D channel range (low channel, high channel).

   On Poseidon, the channel numbers range from 0 to 31. Some channel numbers may not be available, depending on the single-ended/differential configuration mode as explained on page 11. D uring interrupt-based A/D conversions, the channels being sampled must be consecutive in number. To sample only a single channel, set the low channel and high channel to the same channel number. To sample a range of channels, set the low and high channels accordingly.

2. Input voltage range.

   During interrupt-based A/D conversions, the input voltage range must be the same for all channels. Select the input range from the list of codes found in the Analog Input Ranges and Resolution section of this document. This parameter is set with the function *dscADSetSettings()* prior to calling *dscADSampleInt()*.

3. A/D Clock source, internal or external.

   For internal clocking, the on-board 32-bit counter/timer is programmed to the desired sample rate. For external clocking, the signal EXTCLK/DIN3on I/O header CN13, pin 39, controls sampling. Falling edges on this pin generate A/D conversions. The signal is edge sensitive; holding it low generate one conversion.

4. A/D conversion rate, if using internal clock.

   If internal clocking is selected, provide the desired sample rate in Hz as a floating value. The maximum sample rate is 250,000 per second (maximum A/D operating speed), and the slowest rate is .000024383Hz (100KHz input / 232), or approximately 1 sample every 42,950 seconds (approximately 11.9 hours).

5. External gating enable.

   You may choose to allow an external signal on CN13, pin 46, to control the sampling. When the signal is high, sampling occurs, and when it is low, sampling pauses. External gating works with both internal and external clocking. This pin is connected to a 4.7K pull-up resistor.

6. One-shot vs. recycle mode.

   In one-shot mode, the operation occurs one time and then stops, and the parameter *num_*conversions determines the number of samples taken. In recycle mode, the operation runs repeatedly until you stop the operation by calling *dscCancelOp()*. In this case, the parameter *num_*conversions indicates the size of the memory buffer or array used to store the samples. Once the buffer is filled, the data is stored starting at the beginning again, causing the old data to be overwritten. In this situation, you only have access to the latest number of samples equal to *num_*conversions, and you must read the data out of the buffer before it is overwritten. The function *dscGetStatus()* can be used to indicate the current buffer position, which is the location at which the next data value will be stored.

Analog Output Ranges and Resolution

Description

Poseidon uses a 4-channel 12-bit D/A converter (DAC) to provide four analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB. The theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve.

> **Note: In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from the Poseidon computer hardware to an analog signal terminating at an external source.**

Resolution

The resolution is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, so this change is referred to as 1 least significant bit (1 LSB). The value of this LSB is calculated as follows.

1 LSB = Output voltage range / 4096

The maximum voltage swing is defined as the difference between the highest nominal output voltage and the lowest output voltage. For an output range of 0-10V or +/-5V, the maximum voltage swing is 10V.

Example:

For, Output range = ±5V;

Maximum voltage swing = 10V

Therefore,

1 LSB = 10V / 4096 = 2.44mV

Full-scale Range Selection

The D/A converter chip on Poseidon requires two references, one for the low end and one for the high end of the range. The high end can be set to 5V, 10V, or Programmable, and the low end can be either 0V (for unipolar output ranges) or minus the high-end voltage. All channels are set to the same output range.

On power up, the D/A automatically resets to mid-scale, which is 0V in bipolar mode and 1/2 full-scale voltage in unipolar mode.

Digital-to-Analog Conversion

This section describes the steps involved in generating an analog output (performing a D/A conversion) on a selected output channel using direct programming, without the driver software.

Perform an D/A conversion according to the following steps. Each step is discussed in detail, below.

1. Compute the D/A output value for the desired output voltage.
2. Compute the LSB and MSB values.
3. Add the channel number to the MSB.
4. Set D/A Simultaneous Update bit.
5. Write the LSB and MSB to the board.
6. Monitor the DACBUSY status bit.

Compute the D/A Output Value for the Desired Output Voltage

A different formula is required for bipolar and unipolar output ranges.

> **Note: The DAC cannot generate the actual full-scale reference voltage, which would require an output code of 4096 that is not possible with a 12-bit number. The maximum output value is 4095. Therefore, the maximum possible output voltage is 1 LSB less than the full-scale reference voltage.**

Unipolar Mode D/A Formula

Output value = (Output voltage) / (Full-scale voltage) * 4096

Example:

Desired output voltage = 2.168V, full-scale voltage = 5V, unipolar mode (0-5V)

Output code = 2.168V / 5V * 4096 = 1776

Bipolar Mode D/A Formula

Output value = (Output voltage) / (Full-scale voltage) * 2048 + 2048

Example:

Desired output voltage = -2.168V, full-scale voltage = 5V, bipolar mode (±5V)

Output code = -2.168V / 5V * 2048 + 2048 = 1160

Compute the LSB and MSB Values

Use the following formulas to compute the LSB and MSB values.

LSB = (D/A Code) AND 255. Keep only the low 8 bits

MSB = int((D/A code) / 256). Strip off low 8 bits, keep 4 high bits

Example:

Output code = 1776

LSB = 1776 AND 255 = 240 (F0 Hex)

MSB = int(1776 / 256) = int(6.9375) = 6

(In other words, 1776 = 6*256 + 240)

Add the Channel Number to the MSB

The channel number is 0-3 and must be inserted in bits 7-6 of the D/A MSB byte, written to Base+5.

Example:

MSB = MSB + Channel * 64

Set D/A Simultaneous Update Bit

To update the DAC, set DASIM bit to 0. This performs an update of the current channel and all previously latched channels, causing a simultaneous update. If no other channels were previously latched, this only updates the current channel. To latch the channel set DASIM bit to 1.

Update example:

MSB = MSB & 0xDF

Latch example:

MSB = MSB + 32

Write the LSB and MSB to the Board

The LSB is written to Base+4 and the MSB/channel no. is written to Base+5. If you are using enhanced features be sure to enable enhanced features before writing to the registers.

Monitor the DACBUSY Status Bit

DACBUSY = 1 for 10µS while the data in registers Base+4 and Base+5 are serially shifted into the D/A chip. After DACBUSY returns to 0 you can write to register Base+4 and Base+5. Registers Base+4 and Base+5 should NOT be written to while DACBUSY = 1. When updating multiple channels for simultaneous update repeat steps 1 to 6, as shown in the following example.

Example:

1. Compute D/A code.

   Using the bipolar mode formula, we compute D/A code = 3V / 5V * 2048 + 2048 = 3276.8.

   Round this up to 3277. (Binary value = 1100 1100 1101)

2. Compute LSB and MSB.

   LSB = 3277 & 255 = 205 (Binary value = 1100 1101)

MSB = int(3277/256) = 12 (Binary value = 1100)

3. Add channel number to MSB.

   MSB = 12 + 1 * 64 = 76

4. Check DASIM. For non-simultaneous update DASIM = 0, for latching DASIM = 1.

   To update: MSB = MSB & 0xDF

   To latch: MSB = MSB + 32

5. Write LSB and MSB to board, enable enhanced features if using latching.

```
outp(Base + 8, 3);     //select page 3
outp(Base + 15, 0xA6); //enable enhanced features
outp(Base + 4, LSB);
outp(Base + 5, MSB);
```

6. Monitor DACBUSY bit, Base + 4 bit 7.

```
while (inp(Base + 4) & 0x80);
```

Waveform Generator

Description

Page 5 of the upper I/O map provides control for the D/A waveform generator. The D/A waveform generator uses an in-FPGA memory block of 1024 words to store D/A codes. The FPGA parses through this memory at a user-programmable speed (or through manual/external trigger) while sending codes to the D/A converter. The generator automatically stops if enhanced features are disabled.

The generator works on frames. A new frame is triggered from a programmable source (manual, counters, external, etc.). For each frame, the FPGA sends a programmable (1, 2 or 4) number of D/A codes from the generator's memory bank to the DAC. This transfer is done in latched mode and the DAC is updated after all codes in a frame are sent. The generator continues this process, incrementing through the memory until it reaches the end of the buffer or reaches a programmable depth, where it wraps back to the beginning of the buffer and continues operation. The generator can be paused, resumed or reset to the beginning of the memory bank at any time.

With the use of the memory block the D/A waveform generator can output consistent waveforms at a maximum frequency of 100KHz. There are four different input sources available for the D/A waveform generator.

- manual software trigger
- counter 0 output
- counters 1+2 output
- external trigger

The memory block also allows a programmable depth which when hit, will wrap and return to the beginning. The threshold ranges from 64 to 1024 and is programmable in multiples of 64.

Programming the D/A Waveform Generator

This section details how to program the D/A waveform generator through direct I/O without using the Diamond Systems driver software. Please, note that the D/A waveform generator is an enhanced feature and enhanced features must be enabled to access the feature.

The following steps, described in the following subsections, are used to programming the D/A waveform generator.

1. Enable enhanced features
2. Reset D/A waveform pointer
3. Latch D/A value
4. Store D/A values into buffer
5. Setup D/A wave form settings
6. Start D/A waveform generator

Enable Enhanced Features

Enable enhanced features as described in the Enabling Enhanced Features section of this document.

Reset D/A Waveform Pointer

Reset the D/A waveform pointer by accessing Page 5, Base+15, bit 2. Writing a 1 to this bit, causing the pointer to start at the beginning, address 0.

Latch D/A Value

The procedure for latching a D/A value is nearly identical to the formula in the Generating An Analog Output section of this document; the only difference is that instead of setting DASIM to 1, set DAGEN to 1. The D/A value code must be computed for the desired voltage. From the computed value, obtain the LSB and MSB and add the

channel number and set DAGEN bit. Write final the LSB and MSB to registers Base+4 and Base+5. By setting the DAGEN bit to 1, the D/A value written will be latched to internal memory instead of the DAC chip.

Store D/A Values into Buffer

Once the D/A code is latched, it must be stored in the waveform buffer. Set Page to 5 and write the buffer address (0 to 1023) for the latched D/A value into Base+12 and Base+13. When Base+13 is written, the latched D/A value at Base+4 and Base+5 is loaded and stored into the waveform memory. Both the D/A output code and D/A output channel are stored.

Setup D/A Wave Form Settings

D/A waveform settings include input source, number of code per frame and threshold. Each can be individually set, in any combination.

There are four different input sources to choose from.

- manual/software trigger
- counter 0 output
- counters 1+2 output
- external trigger

Manual trigger should be used when the rate is slow or inconsistent and needs be controlled in software. Counter 0 output should be used when a consistent rate is desired and counter 1/2 is used for A/D interrupts. Counter 1+2 should be used when a consistent rate is desired and counter 0 is used for other interrupt functions, or if you want to synchronize the waveform generator to A/D interrupt functionality. External trigger should be used when an external signal is desired to generate D/A waveform. Input source is set on Page 5, Base+14, bits 0 and 1.

The number of the code per frame determines the number of buffer values that will be output per frame. Each code is determined by the value set at its address.

For example, if the codes per frame option is set at 2, the first frame will output the codes at address 0 and 1, then 2 and 3, then 4 and 5 and so on. The number of the code per frame is set on Page 5, Base+14, bits 2 and 3.

Threshold determines the number of the code to output before the pointer starts over. The threshold must be set in multiples of 64 up to 1024. When the threshold is reached, the pointer wraps to the beginning. Threshold is set on Page 5, Base+14, bits 4, 5, and 6.

Start D/A Waveform Generator

Initialize D/A waveform output by writing 1 to Page 5, Base + 15, bit 0. The generator continues to output the periodic waveform until you disable it.

Auto-calibration

Poseidon features automatic calibration of both analog inputs and outputs. The potentiometers, which are subject to tampering, vibration, and maladjustment, have been completely eliminated. Instead, all calibration adjustments are performed using an octal 8-bit TrimDAC and precision, low-drift reference voltages on the board. The optimum TrimDAC values for each input range are stored in an EEPROM and recalled automatically on power up. Poseidon also has the A/D auto-calibration algorithm programmed into the dsPIC, featuring a fast, autonomous auto-calibration.

To calibrate the board through software a calibration utility program and software driver function enables you to calibrate the analog inputs and outputs at any time for any range and store the settings in the EEPROM. This feature dramatically improves the accuracy and reliability of the board, since you can calibrate the board as often as desired without worrying about temperature or time drift.

On the analog outputs, the full-scale output range is programmable to any voltage up to 10V, and the board will calibrate to the programmed range. The analog outputs are fed back to the A/D converter so that they can also be calibrated without user intervention.

Background

The Poseidon auto-calibration circuit uses an octal 8-bit TrimDAC IC to provide small adjustments to the offset and gain at various points in the circuit. Four of the DACs are used for the A/D calibration, and the other four are used for the D/A. The 8-bit TrimDAC values are stored in an on-board EEPROM and are recalled automatically on power-up.

An on-board ultra-stable +5V reference chip with 5ppm offset drift is used as the voltage reference for all calibration operations. From this reference several intermediate values are derived that are used for the calibration. One is just under +5V, and one is just above 0V. These values are measured at the factory, and their values are stored in the on-board EEPROM for use by the calibration program. Note that the actual values of the reference signals does not matter, as long as they are stable, since the calibration routine knows the values and can adjust the calibration circuit to achieve them. An extra input multiplexor chip is used to feed the calibration voltages into the A/D circuit during the process.

For bipolar A/D calibration, first 0V is measured, then the TrimDAC is adjusted until the target A/D reading is achieved. For unipolar calibration, the voltage just above 0 is used as the first measurement value. Two TrimDAC channels are used for the offset. The first channel provides a coarse adjustment to bring the A/D readings into range, and the second channel provides a fine adjustment for maximum accuracy. The use of both coarse and fine adjustments provides a wider range of total adjustment capability. The range of the fine adjustment exceeds the smallest change in the coarse adjustment, so there is no gap in the adjustment range.

After the offset is adjusted, the full-scale is adjusted in a similar manner. The reference value just under 5V is fed into the A/D, and two additional TrimDACs provide coarse and fine adjustments to achieve the target A/D near-full-scale reading.

Once the A/D is completely calibrated, the 12-bit D/A channels can be calibrated. Unlike the A/D circuit, which uses a single A/D for all input channels, the D/A circuit actually contains a single D/A converter for each of the four output channels. These channels are fed into the calibration multiplexor and the remaining four TrimDAC channels are used to calibrate them in a similar manner to the A/D. A single adjustment is used for the high reference, and both coarse and fine adjustments are used for the low reference.

The entire process takes about one second for each input range. Once it is complete, the board is ready to run. All eight TrimDAC values are stored in the EEPROM so that the next time power is cycled to the board, the values will be loaded automatically.

Performing Auto-calibration with Software

The Universal Driver™ software provides two functions, *dscADAutocal()* and *dscDAAutocal()*, which can be called from within a user program to calibrate the board at any time. In addition, a standalone DOS program, *DMM32CAL.EXE*, is provided to enable calibration without requiring any programming.

Performing Auto-calibration with dsPIC

Poseidon has an onboard microprocessor that can perform auto-calibration for you, automatically. The microprocessor can be configured to trigger calibration because of temperature changes, or it can be manually triggered by software.

Temperature-triggered auto auto-calibration is enabled by writing a 1 to Page 4, Base+14, bit 3 (ACREL). When this bit is set, the Autocal holdoff line is released. The dsPIC monitors temperature changes and auto-calibrates the board every 5ºC.

If more control over auto auto-calibration is desired, set the ACHOLD bit to stop the temperature trigger (this is the default state), and use the ACTRIG bit to engage auto-calibration when desired.

While the dsPIC is running auto auto-calibration, Base+4, bit 5, ACACT will be high. Users should monitor this bit whenever they have enabled auto auto-calibration. While the dsPIC is auto-calibrating, user software may not interact with the A/D circuit. When performing regular A/D functions, users should set the ACHOLD bit high to turn off auto auto-calibration.

Digital I/O Operation

Poseidon contains two sets of digital I/O lines.

- An internal 82C55-type digital I/O circuit provides 24 digital I/O lines that emulate the function of Mode 0 of an 8255 chip. These lines are buffered to provide extra drive current in output mode, and are available on digital I/O header, CN12.
- Digital I/O header CN13 also contains auxiliary digital I/O. Four inputs and three outputs can be used for general purpose DIO as long as they are not used for any special functions.

Main Digital I/O Internal 82C55 Circuit

The 82C55-type digital I/O circuit is accessed through page 1 at addresses Base+12 through Base+15. For example, address 0 on the chip is equivalent to address 12 in the register map. Before performing any access to the digital I/O circuit, you must set the current page to page 1 using the miscellaneous control register at Base+8, to ensure that the proper page is enabled.

> **Note: that writing page bits to the miscellaneous control register will not cause a board reset or interrupt reset operation as long as the two reset bits are left at 0. Also, writing a 1 to either reset bit in this register will not change the contents of the page bits.**

The current page may be determined by reading the page bits at Base+7.

This digital I/O circuit functions like an 82C55 in Mode 0, direct I/O, or Mode 1, latched I/O. In Mode 1, latch and acknowledge signals are provided. Each port, A, B and C, can be programmed for input or output. Port C can also be split into two halves, with each half programmed for a different direction.

All 24 lines have 10KΩ resistors connected to them that can be configured for either pull-up or pull-down operation. In addition, all lines are buffered by 74FCT245 line drivers between the controller chip and the I/O header. These line drivers change direction automatically in response to the control word written.

On power up, all ports are set to input mode and can be used as inputs immediately. Before using any port as an output, the port direction register must be programmed appropriately.

The following table provides a list of common configuration register values for programming port direction.

Value	*Port A*	*Port B*	*Port C*
9Bh	Input	Input	Input
92h	Input	Input	Output
99h	Input	Output	Input
90h	Input	Output	Output
8Bh	Output	Input	Input
82h	Output	Input	Output
89h	Output	Output	Input
80h	Output	Output	Output

Mode 0 Digital I/O

This is the simpler of the two I/O modes and works well for most uses. In mode 0, the handshaking signals Latch and Acknowledge are not used. When reading any port in input mode, the data at the I/O pins at the time of the read command is returned.

Mode 1 Digital I/O With Handshaking

In Mode 1, a Latch input and an Acknowledge output signal are provided for handshaking operation. This allows the external circuit to tell the board when new input data is ready or when it has accepted the current output data, and it allows the board to tell the external circuit when it has read the current input data and when new output data is ready. Only Port A may be operated in Mode 1.

In all cases, the starting/resting conditions are Latch input = low, and Acknowledge output = low.

Note: Mode 1 is not currently supported by Diamond Systems Universal Driver software.

Auxiliary Digital I/O

CN12 contains three digital outputs and four digital inputs that can be used either for general purpose digital I/O, or for A/D and counter/timer functions. The operation of these bits is controlled with various bits in two control registers.

Outputs

DOUT2/CTROUT2, CN12 pin 28

The function of this pin is determined by OUT2EN, Base+10 bit 5.

DOUT1/SHOUT CN12, pin 30

This pin is always the value written to DOUT1 at Base+1, bit 1.

DOUT0/CTROUT0 CN12, pin 27

The function of this pin is determined by OUT0EN, Base+10, bit 4.

Inputs

DIN3/EXTCLK CN12, pin 31.

This signal may always be read at Base+4, bit 3. It may function as an external clock to control A/D conversion timing when CLKEN = 1 and CLKSEL = 0, in Base+9.

DIN2/EXTGATE CN12, pin 32.

This signal may always be read at Base+4, bit 2. It may function as an external gate to enable and disable A/D conversions when GT12EN = 1, in Base+10, bit 0.

DIN1/GATE0 CN12, pin 26.

This signal may always be read at Base+4, bit 1. It may function as an external gate for Counter 0 when GT0EN = 1 in Base+10, bit 2. When used as a gate, it is active high, which means that Counter 0 counts as long as it is high and does not count when it is low.

DIN0/CLK0 CN12, pin 25.

This signal may always be read at Base+,4 bit 0. It may function as an external clock for counter 0 when SRC0 = 0 in Base+10, bit 1. When used as a clock for Counter 0, the rising edge is active.

Counter/Timer Operation

Counter/Timer Features and Configuration Options

Poseidon emulates an 82C54 counter/timer chip, providing 3 16-bit counter/timers.

Counters 1 and 2 are cascaded together to form a 32-bit counter/timer for use as a programmable A/D sampling clock. The output of counter 1 provides the input for counter 2, and the output of counter 2 is fed to the A/D triggering circuit as well as the I/O header CN12. If not being used for A/D sampling, these counter/timers may be used for other functions. Counter/timer 0 is always available for user applications.

The inputs of the counter/timers are programmable, and the outputs may be routed to the I/O header under software control. The table, below, lists the key features of each counter/timer.

Counter	*Input*	*Gate*	*Output*
0	• 10MHz on-board • 10KHz on-board • DIN0/CLK0 (CN12, pin 25)	DIN1/GATE0 (CN12, pin 26)	DOUT0/CTROUT0 (CN12, pin 27)
1	• 10MHz • 100KHz	DIN2/EXTGATE (CN12, pin 32)	Not available
2	• Counter 1 out	DIN2/EXTGATE (CN12, pin 32)	• DOUT2/CTROUT2 (CN12, pin 28) • Used internally for A/D sampling control

Counter/Timer Configuration

The counter/timer configuration is determined by the control register at Base+10. Note that the outputs of counters 0 and 2 are routed to pins on I/O header CN12 under software control rather than being hardwired.

Configuring the A/D sampling clock is done with the control register at Base+9. Bit CLKEN selects whether or not the A/D hardware clocking is enabled. If clocking is enabled, bit CLKSEL selects whether or not it is the output of counter/timer 2 or the external clock input at DIN3/EXTCLK, on CN12.

Counter/Timer Access and Programming

Before performing any access to the chip, you must set the current page to page 0 with the miscellaneous control register at Base+8 to ensure that the proper page is enabled. Note that writing page bits to the miscellaneous control register does not cause a board reset or interrupt reset operation as long as the two reset bits are left at 0. Also, writing a 1 to either reset bit in this register does not change the contents of the page bits.

The current page may be determined by reading the page bits at Base+7.

Once you write the proper page value, you can read and write to the 82C54 registers.

Watchdog Timer Programming

A software trigger relies on a thread of execution to constantly trigger watchdog timer. If the thread is ever halted, the timer decrements to zero and the board resets. The timer may be programmed from zero to three seconds, in 0.2 second intervals.

The registers described below are used to program the watchdog timer. The register set is located at a base address of 258h.

Watchdog Timer Register Set			
Base +	***Address***	***Write Function***	***Read Function***
4	25Ch	Watchdog Trigger	-
5	25Dh	Watchdog Configuration	Watchdog Configuration Read-back
7	25Fh	Watchdog Enable	Watchdog Status

Watchdog Trigger: Base+4 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	WDTRIG	-	-	-	-

WDTRIG Writing a one to this bit triggers the watchdog timer.

Watchdog Configuration: Base+5 (Read/Write)

Bit:	7	6	5	4	3	2	1	0
Name:	WDT3	WDT2	WDT1	WDT0	-	-	-	-

WDT3-0 Watchdog timer reload value. Each internal clock tick decrements the watchdog counter by one from this value. A tick interval is 0.2 seconds.

Watchdog Enable: Base+7 (Write)

Bit:	7	6	5	4	3	2	1	0
Name:	WDEN7	WDEN6	WDEN5	WDEN4	WDEN3	WDEN2	WDEN1	WDEN0

WDEN7-0 Writing 0x99 to this register enables and loads the watchdog timer with the value in the Base+5 register. Writing any other value to this register disables the watchdog timer.

Watchdog Status: Base+7 (Read)

Bit:	7	6	5	4	3	2	1	0
Name:	-	-	-	WDST	-	-	-	-

WDST Watchdog status:
0 = disabled.
1 = enabled.

Program the watchdog timer according to the following steps.

1. Enable the watchdog timer by writing 99h to Base+7. This causes the timer to be reloaded with the value of WDT3-0 in Base+5 and starts the internal counter.
2. When the watchdog is enabled and the internal counter is running, keep the watchdog from expiring by setting the WDTRIG bit in Base+4. This reloads the counter with the value in Base+5. If the counter reaches zero, watchdog circuitry pulses the reset line and disables the watchdog timer.
3. Disable the watchdog timer at any time by writing any value other than 99h to Base+7.

FlashDisk Module

Poseidon is designed to accommodate an optional solid-state FlashDisk module. This module contains 128MB, 256MB, 512MB, 1GB, 2GB, or 4GB of solid-state non-volatile memory that operates like an IDE drive without requiring additional driver software support.

Model	*Capacity*
FD-128-XT	128MB
FD-256-XT	256MB
FD-512-XT	512MB
FD-1G-XT	1GB
FD-2G-XT	2GB
FD-4G-XT	4GB

Figure 26: FlashDisk Module

Installing the FlashDisk Module

The FlashDisk module installs directly on the IDE connector, CN2, and is held down with a spacer and two screws onto a mounting hole on the board.

For master mode, install the jumper on pins 3 and 4. For slave mode, install the jumper on pins 1 and 2.

Exit the BIOS and save the change. The system will now boot and recognize the FlashDisk module as drive *C:*.

Using the FlashDisk with Another IDE Drive

The FlashDisk occupies the board's 44-pin IDE connector and does not provide a pass-through connector. To utilize both the FlashDisk and a notebook drive, the ACC-IDEEXT adapter and cables are required.

Power Supply

The 44-pin cable carries power from the CPU to the adapter board and powers the FlashDisk module and any drive using a 44-pin connector, such as a notebook hard drive.

A drive utilizing a 40-pin connector, such as a CD-ROM or full-size hard drive, requires an external power source through an additional cable. The power may be provided from the CPU's power out connector, J12, or from one of the two 4-pin headers on the ACC-IDEEXT board. Poseidon cable no. 6981006 may be used with either power connector to bring power to the drive.

FlashDisk Programmer Board

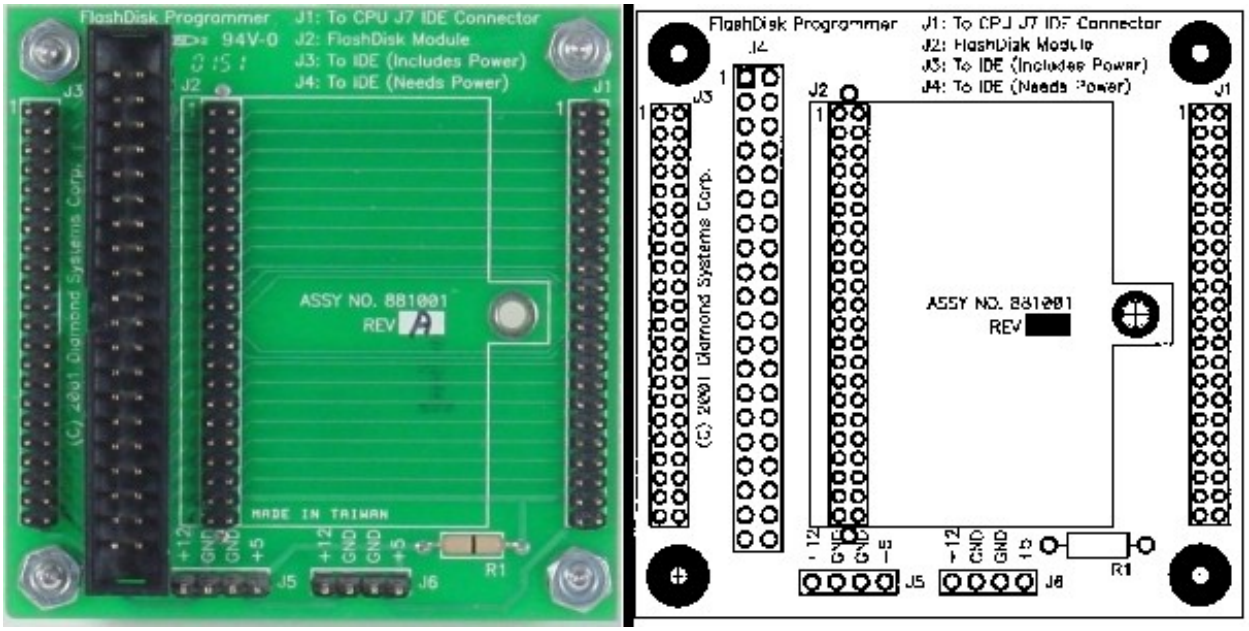
The FlashDisk Programmer Board accessory, model no. ACC-IDEEXT, may be used for several purposes. Its primary purpose is to enable the simultaneous connection of both a FlashDisk module and a standard IDE hard drive or CD-ROM drive, to allow file transfers to/from the FlashDisk. This operation is normally done at system setup. The board can also be used to enable the simultaneous connection of two drives to the CPU.

Connector J1 connects to the IDE connector on Poseidon with a 44-pin ribbon cable (part no. 6981004). Both 40-pin 0.1-inch spacing, J4, and 44-pin 2mm spacing, J3, headers are provided for the external hard drive or CD-ROM drive. A dedicated connector, J2, is provided for the FlashDisk module. Any two devices may be connected simultaneously using this board with proper master/slave jumper configurations on the devices.

The FlashDisk Programmer Board comes with a 44-wire cable no. (DSC no. 6981004) and a 40-wire cable no. (DSC no. C-40-18) for connection to external drives. The FlashDisk module is sold separately.

The 44-pin connector (J1, J2 and J3) and mating cable carry power, but the 40-pin connector (J4) and mating cable does not. Connectors J5 and J6 on the accessory board may be used to provide power to a 44-pin device attached to the board when the board is attached to a PC via a 40-pin cable. These headers are compatible with a standard PC internal power cable.

Figure 27: FlashDisk Programmer Board Layout



I/O Cables

For custom installations as well as development, offers the cables listed in the following table.

Cable No.	*Description*
6981072	Analog I/O, IDC40 to IDC40 2mm 12"
6981073	Digital I/O, IDC34 to IDC34 2mm 12"
6981080	Ethernet 1G 2mm to panel
6981081	Serial, 2mm to 2x DB9M
6981082	USB, 2mm to 2x USB
6981083	PS2, 2mm to 2x Mini-DIN
6981084	VGA, 2mm to DD15F
6981085	Audio, 2mm to 3x 3.5mm
6981087	Poseidon Speaker Out
6981088	Poseidon Utilities
6981091	Poseidon Power In

Mounting PC/104-*Plus* Cards onto a Poseidon Baseboard

Poseidon is designed to serve as a baseboard for a stack of PC/104 or PC/104-*Plus* boards. Up to four PC/104-*Plus* boards are supported. Any PC/104 boards should be mounted on top of the PC/104-*Plus* board stack, when both board types are to be combined.

PC/104-*Plus* requires a board configuration setting for each board in a PC/104-*Plus* board stack. Ensure that the lowest board in the stack is assigned to the lowest board ID, as per the PC/104-*Plus* specification. This setting establishes the PCI Clock, PCI Interrupt routing, the Bus Master signals, and the device ID setting for PCI configuration. These settings are critical. Two boards should never be configured with identical board stack settings, because this will result in problems accessing PCI devices and may cause damage to the main board and/or the PC/104-*Plus* boards in the stack.

Note: Do not configure two PC/104-*Plus* boards with the same board stack ID!

PC/104 is much less critical in this regard, but care should be taken to ensure that the ISA resource allocations allow space for the specific boards added in the stack. Resources (IRQs, in particular) can be very limited in a system with so many devices present on the main board. It is important to ensure that ISA I/O, Memory, IRQ, and DMA configuration conflicts are resolved before powering-up the system. Otherwise, it is possible that the system boot sequence will be impeded by these conflicts.

Take care to read through this documentation, particularly the section on ISA Resource defaults, to familiarize yourself with the internal resources used before adding components that might cause conflicts.

When adding boards to the PC/104(+) board stack, be sure to include board standoffs. Inordinate flexing of the main PC/104 and PC/104-*Plus* connectors can seriously reduce the effective lifespan of the connectors, as well as cause potential system instability due to incomplete connection across system buses.

On the 2.0GHz model PSDC2.0, the processor fan interferes with the side connectors of PC/104 boards such as DMM32X or EMM8P. Remove he strain relief from the connector cable to avoid the clearance problem.

PNL-PSD Panel I/O Board for Poseidon CPU

1. Description

PNL-PSD is a panel I/O board designed for the Poseidon CPU board. It provides a cable-free means of installing these CPUs in the enclosure system and attaching standard peripheral devices to the system.

1.1 Reference Documents

The latest version of the following documents should be consulted for additional information to support this product specification:

- Poseidon mechanical drawings
- Poseidon PCB and product specification

1.2 Detailed Feature List

- Contains consumer-type I/O connectors for most Poseidon system I/O
- Contains power input connection
- Contains additional I/O connector for one Mercury Ethernet port
- Optional provision for a panel-mounted power switch
- Optional reset, power on, and PC speaker features

1.3 Indicators

The panel board contains a power-on indicator LED that is visible through the panel of the enclosure. This LED is sourced from the +5VDC of the utility header (switched power).

The panel board contains a provision for a low-cost PCB-mounted PC speaker. The speaker is not installed in the default configuration.

1.4 Jumper Configuration

The panel board contains two configuration jumpers JP1 and JP2.

- **External Power Enable - JP1:** Use a jumper between pins 1 and 2 only if Poseidon is to be powered from an external power supply such as PS-5V-04 via the panel board and power switch emulation is desired. For most embedded applications where no power switch is desired and the board must power on upon applying power, do not connect this jumper, or leave it in the off location by placing it between pins 2 and 3.

  If the panel board is to be used while the SBC is powered of an ATX style power supply using the MOLEX connector (CN9 on Poseidon), JP1 should not have a jumper or the jumper should be between pins 2 & 3.

  Please consult the Poseidon power configuration table on page 35 for complete information on all the different power options.

- **Shutdown Disable - JP2:** Install a jumper in positions 1 & 2 of JP2 to disable the shutdown output control. If the panel board and SBC are to be used with a Jupiter (JMM) power supply with shutdown control, remove the jumper or install a jumper between pins 2 & 3.

2. I/O Connectors

2.1 CPU Connectors

All CPU connectors are mounted on the bottom side of the board and are designed to mate directly with the associated connectors on the CPU board. The vertical length of all bottom side connectors is designed to seat properly with the CPU connectors. All connector pinouts are available in the product user manuals.

The headers on the first row are placed at precise 2mm intervals, so it is possible to use a single, large 2mm female socket to cover multiple features.

First Row Features	Connector type
Power	2x10 pin 2mm female socket
Audio	2x5 pin 2mm female socket
VGA	2x5 pin 2mm female socket
Ethernet	2x5 pin 2mm female socket
USB 0&1	2x5 pin 2mm female socket
USB 2&3	2x5 pin 2mm female socket
Utility	2x4 pin 2mm female socket

Keyboard/Mouse	2x4 pin 2mm female socket
Serial Ports	2x20 pin 2mm female socket

The following CPU connectors and features are not accessible via the panel board:

- SATA and IDE connectors
- PC/104 and PC/104+ bus connectors
- External battery connector
- Output power connector
- LCD and LCD Backlight
- Analog and Digital I/O
- Speaker
- IDE LED

2.2 Topside Serial Header

Serial ports 3 and 4 will be exposed via a 2x10 2mm vertical SMT male header.

DCD 3	1	2	DSR 3
RXD 3	3	4	RTS 3
TXD 3	5	6	CTS 3
DTR 3	7	8	RING 3
Ground	9	10	No Connect
DCD 4	11	12	DSR 4
RXD 4	13	14	RTS 4
TXD 4	15	16	CTS 4
DTR 4	17	18	RING 4
Ground	19	20	No Connect

2.3 Topside USB Header

USB ports 2 and 3 are brought out to two locations, a front panel industry-standard dual-port connector and a topside pin header. The topside pin header is a 2x5mm header that mirrors the pinout of the connector on Poseidon.

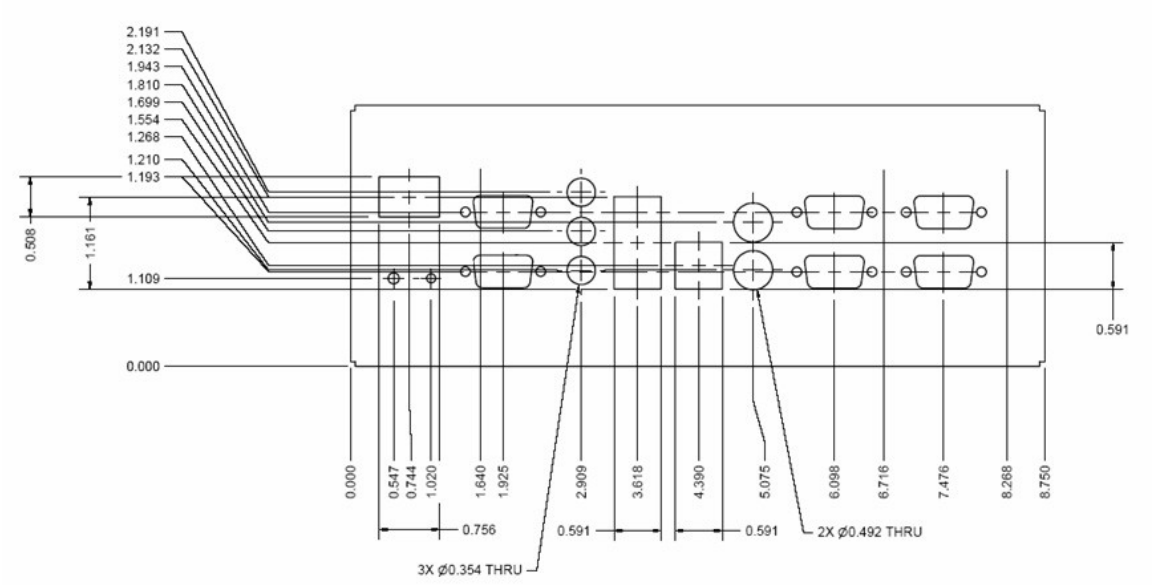
2.4 Topside Utility Header

The 2x4 Poseidon utility header should be mirrored on the topside using a 2x4 2mm SMT male pin header.

2.5 User I/O Connectors

All user I/O connectors are mounted on the top side of the board and are accessed through openings in the front panel of the enclosure. All I/O connectors provide a firm latching method wherever possible. All connectors should be aligned such that their faces are coplanar 0.05" from the lower edge of the board. All DSUB connectors should use 4-40 inserts (screwlocks will be provided separately). All connectors should be spaced apart enough to avoid interference when inserting mating connectors in adjacent connectors.

Feature	Connector type
Serial ports	1x dual stacked male DB9 male connectors (2 ports total)
Keyboard and Mouse	Standard dual stacked PS/2 female sockets
Ethernet and USB	1x (Ethernet + dual USB) stacked connector; 1x dual USB only stacked connector
Video	Standard DB15 high density female
Audio	Stacked mic, line in, line out (use standard jack colors)
Power	DB9 female



2.6 Reset Switch

The reset switch is a momentary switch that is accessible only through a small hole that can accommodate a paper clip.

2.7 DC/DC Power I/O

The Panel board will interface with an internal DC/DC converted using two connectors.

A 1x6 0.156" straight friction lock header will carry the variable power input (ref. Molex 26-48-1065).

1	Variable Power Input
2	Variable Power Input
3	Ground

4	Ground
5	Variable Power Input
6	Ground

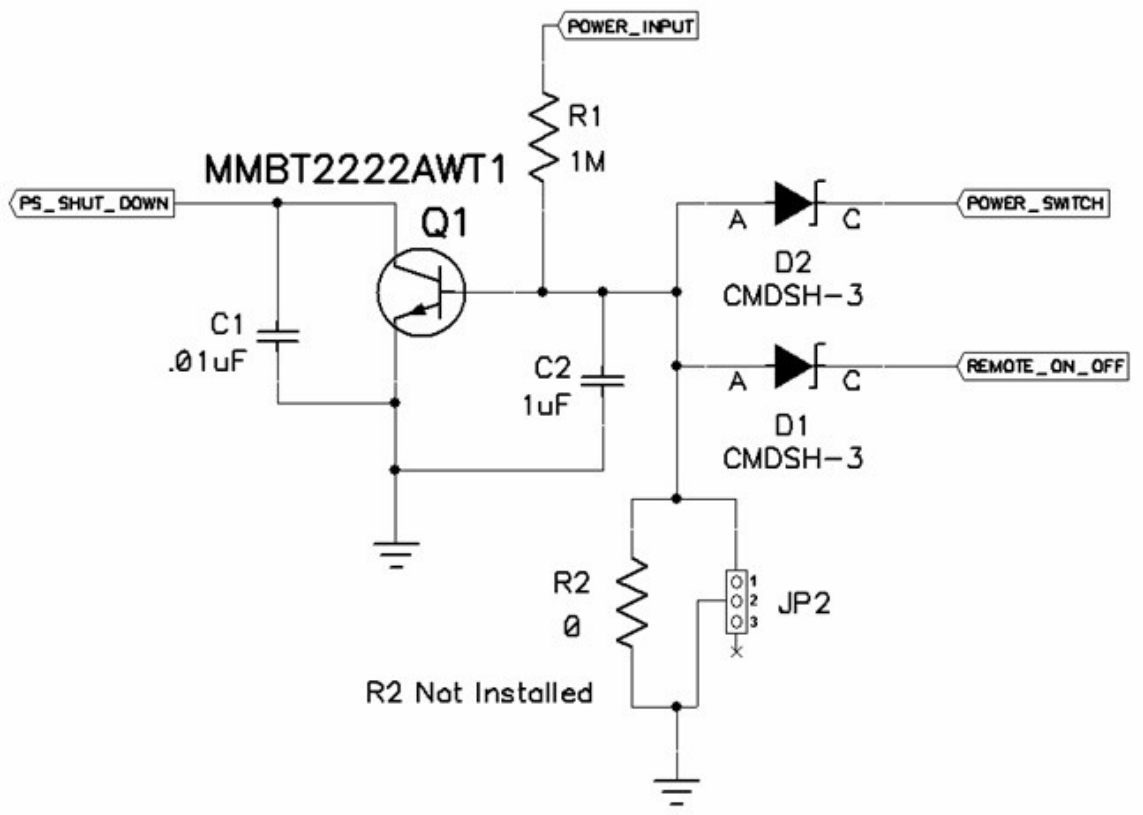
A 1x2 0.1” straight friction lock header will carry the shutdown signals (ref. AMP/Tyco Electronics part # 640456-2).

1	PS Shut Down
2	Ground

2.8 Power Supply Shut Down Circuit

This circuit is required to make the panel compatible with our Jupiter series power supply.

PS_SHUT_DOWN	Connect to ‘PS Shut Down’ on internal headers
POWER_INPUT	Connect to Variable Power Input line
POWER_SWITCH	Connect to pin 3 of the Poseidon utility header
REMOTE_ON_OFF	Connect to pin 20 of the Poseidon power header



3. Front Panel Connectors

3.1 Keyboard and Mouse

The keyboard / mouse connectors are 6-pin female mini-DIN connectors using the industry standard pinout.

1	Data
2	NC
3	Ground
4	+5V
5	Clock
6	NC

3.2 Ethernet

The Ethernet connector is a 8-pin RJ-45 jack using the industry-standard pinout for 100BaseT.

3.3 Serial ports

Serial ports 1 and 2 are implemented with 9-pin male Dsub connectors. Each connector has the following pinout. The RS-232 pinout is industry-standard DTE, while the RS-422/485 pinouts are DSC standard

Pin	RS-232	RS-422 (ports 3-4 only)	RS-485 (ports 3-4 only)
1	DCD	NC	NC
2	RXD	TXD+	TX/RX+
3	TXD	Ground	Ground
4	DTR	RXD+	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	TXD-	Tx/RX-
8	CTS	RXD-	NC
9	RI	NC	NC

3.4 USB

The 4 USB connectors use the industry standard pinout. The connector shield is connected to the shield pins of the CPU connectors. Ports 0 and 1 connect to the combination USB/Ethernet connector. Ports 2 and 3 go to a 2-port USB connector on the panel and a 2x5 pin header for internal use (see above).

1	Pwr +
2	Data -

3	Data +
4	Pwr -

3.5 VGA

The VGA connector is a 15-pin high-density female Dsub connector using the industry-standard pinout.

1	Red
2	Green
3	Blue
4	NC
5	NC
6	Red Gnd
7	Green Gnd
8	Blue Gnd
9	NC
10	NC
11	NC
12	SDA
13	Hsync
14	Vsync
15	SCL

3.6 Power Input

The input power connector is a DB9 female connector with connections for +5VDC input and also a variable DC voltage input. Only one of these inputs is used at a time. +12V may also be provided via this connector for use by an LCD backlight.

1	+5V
2	+5V
3	Gnd
4	Vin
5	+12V
6	+5V
7	Gnd
8	Gnd
9	Vin

4. Mechanical Requirements

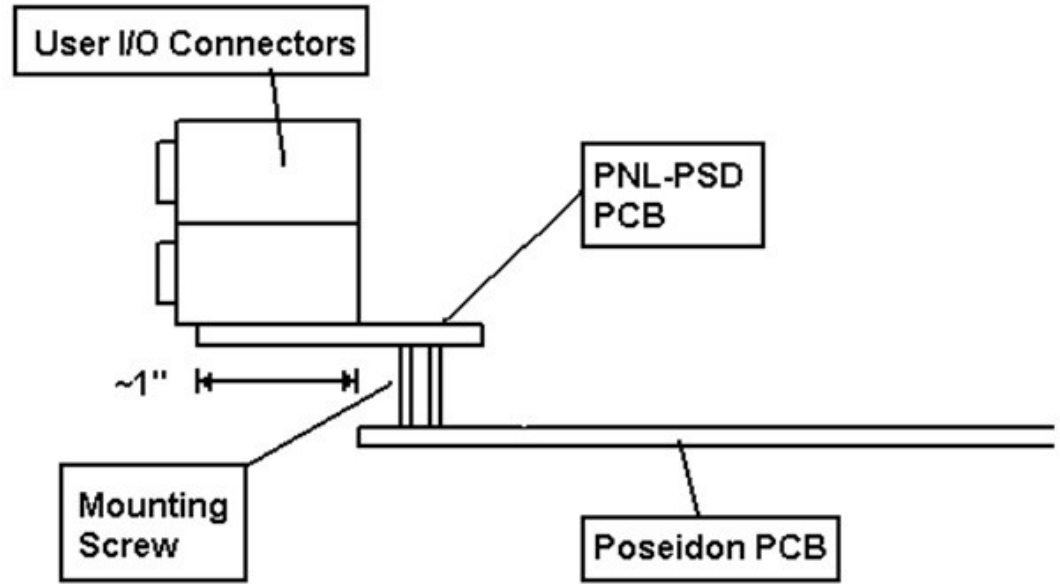
4.1 Orientation

The board is installed along the lower edge of the Poseidon where the system I/O headers are located. The panel's PCB will be parallel to the Poseidon PCB.

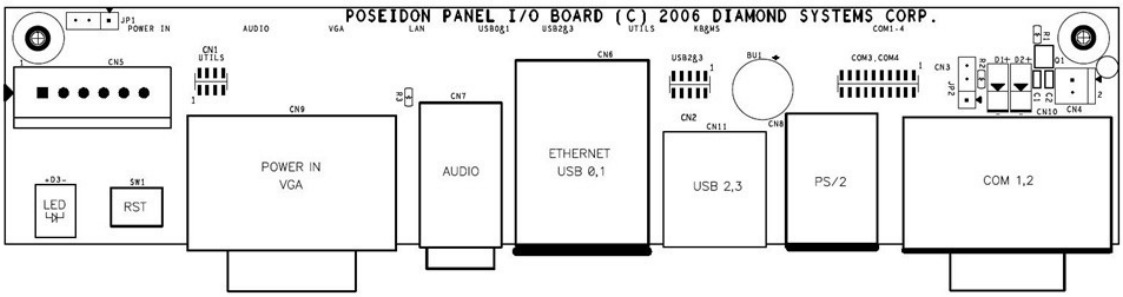
The panel board may extend 1" from the lower edge of the Poseidon to support the external headers. It will extend no further than required to support the connectors along the lower edge of the Poseidon.

The panel must not interfere with the speaker, digital I/O or analog I/O headers on the Poseidon board.

Side view (artist's rendering):



Overhead view:



4.2 Mounting Hardware

The panel board ships with a hardware kit consisting of two male/female spacers with 4-40 threads and two 4-40 x 1/4 panhead Phillips screws.

Customization Options

There are many customer-specific customizations that can be done for the Poseidon, including:

- Latching connectors (replacing the box headers used for most of the board I/O connections).
- Connectors with extra gold contact plating.
- Alternative heatsinks for low air-flow and dusty environments.
- Conformal Coating.
- Jumperless configuration (all settings made on-board with no jumper headers required).

Contact your sales representative for details on these special-order options.

Specifications

CPU

Processor	VIA Eden ULV	VIA C7
CPU Speed	1.0GHz	2.0GHz
CPU Power Consumption	3.5W	15W
Cooling	Heat sink, no fan	Heat sink + fan
Operating Temperature	-40 to +75ºC	-40 to +75ºC

- Chipset: VIA CX700
- Front Side Bus: 400MHz
- SDRAM memory: 512-1024MB 533MHz DDR2 soldered on-board
- Bus interface: PC/104-Plus (ISA + PCI)
- Display type: CRT and / or 24-bit dual channel LVDS flat panel
- CRT resolution: 2048 x 1536
- Flat Panel Resolution : UXGA 1600 x 1200
- Video memory: 128MB UMA
- USB ports: (4) USB 2.0
- Serial ports: (2) RS-232 and (2) RS-232/422/485
- Networking: 10-/100-/1000Base T Gigabit Ethernet
- Mass storage interfaces: (1) S-ATA, (1) IDE UDMA 100
- Keyboard/mouse: PS/2
- Audio: AC ’97, Line-in, Line-Out, Mic and amplified speaker interface

Data Acquisition Circuitry

- Analog inputs: 32 single-ended, 16 differential, or 16 SE + 8 DI; user selectable
- A/D resolution: 16 bits
- Bipolar ranges: ±10V, ±5V, ±2.5V, ±1.25V, ±0.625V
- Sample rate: 250KHz maxtotal
- Unipolar ranges: 0-10V, 0-5V, 0-2.5V, 0-1.25V, 0-.625V,
- Input bias current: 100pA max
- Protection: ±35V on any analog input without damage
- Input Impedance: 10^13 ohms
- Nonlinearity: ±3LSB, no missing codes
- Conversion rate: 250,000 samples/sec.max
- On-board FIFO: 1024 samples, programmable threshold
- A/D and D/A Calibration: Automatic using on-board microcontroller and temp sensor
- Analog Outputs: 4, 12-bit resolution
- Output ranges: ±5V, ±10V, 0-5V, 0-10V
- Output current: ±5mA max per channel
- Settling time: 6µS max to 0.01%
- Relative accuracy: ±1 LSB
- Nonlinearity: ±1 LSB, monotonic
- Reset: Reset to zero-scale or mid-scale (jumper selectable)
- Waveform buffer: 1,024 samples
- Digital I/O Lines: 24 programmable direction
- Input voltage Logic: 0: 0.0V min, 0.8V maxLogic 1: 2.0V min, 5.0V max
- Input current: ±1µA max
- Output voltage: Logic 0: 0.0V min, 0.33V maxLogic 1: 2.4V min, 5.0V max
- Output current: Logic 0: 64mA max per lineLogic 1: -15mA max per line
- A/D Pacer clock: 32-bit down counter (2 82C54 counters cascaded)
- Clock source: 10MHz on-board clock or external signal
- General purpose: 16-bit down counter (1 82C54 counter)

Power Supply

- Input Voltage: +5VDC ±5%

General

- Dimensions: 4.528” x 6.496” (115mm x 165mm)
- Weight:
  - PSDE10 - 512N, 8.3 oz.
  - PSDE10 - 512A, 8.6 oz.
  - PSDC20 - 1024A, 9.0 oz.

Additional Information

Additional information can be found at the following websites.

1. Diamond Systems Corporation: http://www.diamondsystems.com/
2. VIA Technologies, Inc. (Processors): http://www.via.com.tw/en/products/processors/
3. VIA Technologies, Inc. (North/South bridge): http://www.via.com.tw/en/products/chipsets/c-series/cx700/

Appendix A. COM3/4/ADC IRQ Configuration for First Release Boards, Rev A1

JP3	
Pin	***Function***
1	IRQ15; selectable for COM4
2	IRQ9; selectable for COM3
3	COM4 select for IRQ
4	COM3 select for IRQ
5	IRQ3; selectable for COM4 or COM3
6	IRQ4; selectable for COM3 or ADC
7	COM3 select for IRQ
8	AD select for IRQ
9	AD select for IRQ
10	IRQ5; selectable for COM3 or ADC
11	IRQ6; selectable for COM3 or ADC
12	COM3 select for IRQ

Technical Support

For technical support, please email support@diamondsystems.com or contact technical support at 1-650-810-2500.